Towards ALD-grown MoS_2 devices for CMOS BEOL

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The achievement of isolated graphene in 2004 [1] by Geim and Novoselov has significantly boosted research in two-dimensional (2D) materials. Among the most promising 2D materials for the next electronic nodes are the transition metal dichalcogenides (TMDs), which present [2]: i) suitable bandgaps to be compatible with CMOS technology, ii) large effective masses reducing source-to-drain tunneling, iii) controllable thicknesses at the atomic level allowing excellent electrostatic control. However, difficulties in their fabrication such as the scarcity of scalable fabrication methods [3] still suppose a bottleneck for their industrial implantation. Despite the synthesis of these materials appearing simple, the use of high-temperature synthesis methods such as chemical vapor deposition (CVD) are forbidden in the direct 2D material growth on top of already processed silicon CMOS circuits. This fact obligates to use a mandatory layer-transfer process after growing the 2D material on a sacrificial substrate. On the other hand, atomic layer deposition (ALD) enables precise control over the thickness of the deposited layers due to a two-phase self-limiting process, conducted at relatively low temperature (100-400ºC). This temperature range is compatible with the back-end-of-line (BEOL) of CMOS technology [4]. Nevertheless, this low temperature may also cause poor crystallization and small grain size in the 2D layer, potentially limiting the carrier mobility and device performance [5].

We present MoS_2 back-gated devices synthesized via ALD through $[(NtBu)_2(NMe_2)_2Mo]$ and H_2S precursors [6]. The process was carried out directly on Si/90nm-SiO_2 wafers (100 mm) controlling the final MoS_2 thickness as a function of the number of cycles at a fixed temperature of 370ºC. The various wafer colors depicted in Figure 1.a are indicative of diverse deposited layer thicknesses and absorbance properties. The confirmation of the synthesized MoS_2 layer was performed through Raman characterization as illustrated in Figure 1.b. The spectrum exhibits three characteristic peaks: one appearing around 509 cm^{-1}, associated with the presence of Si/SiO_2 beneath the MoS_2; and the two peaks corresponding to the in-plane (E_{2g}) and the out-of-plane (A_{1g}) vibrational modes produced by 2H-MoS_2 crystals. Regardless the number of cycles employed in the synthesis, the peaks exhibit a separation of 24 cm^{-1}, indicative of a multi-layer material. In Figure 1.c, the atomic force microscopy topography of an etched device corroborates the presence of an approximately 10 nm-thick MoS_2 layer in a 90-cycles sample. Evaluation of the MoS_2 sheet resistivity was directly carried out through 4-probe characterization without any processing. Sheet resistance divided by the form factor ($F \sim \pi / \ln(2)$) [7] as a function of the synthesis parameters is shown in Figure 1.d suggesting resistivities in the MΩ range. Note that the sample is characterized at zero back-gate bias. Increasing the number of cycles and reducing the synthesis temperatures seems to conduct a material conductivity improvement.

To create back-gated devices, we employed standard photolithography with a metal (Cr/Au) lift-off process and SF_6 selective etching. Unfortunately, due to layer delamination (a common issue with these 2D materials [8]), only few structures were available. Initial electrical characterization of the back-gated devices revealed interestingly symmetrical output characteristic (Figure 2.a) and a prominent p-type branch (Figure 2.b). Significative gate leakage and the absence of photocurrent phenomenon were reported. Additionally, considerable hysteresis in the double gate swept, related to the interface traps,

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were observed. These advances open the door to optimizing the layer thickness and lithography process for scalable and CMOS-compatible ALD-grown MoS_2 transistors.

References

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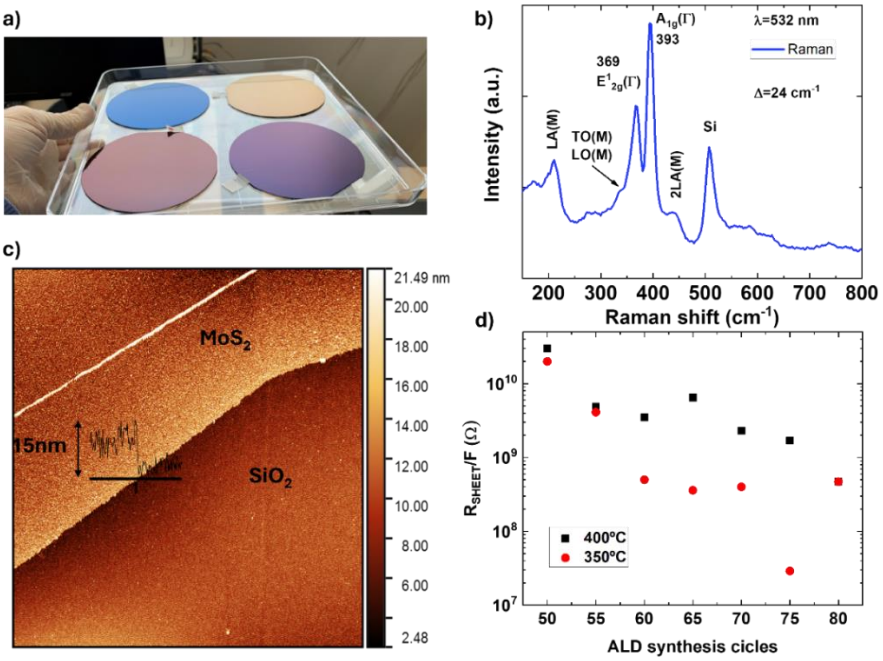

Figure 1: a) ALD-grown MoS_2 layers with increasing number of cycles (from left-bottom corner to left-top corner) on 100mm SiO_2/Si wafers. b) Raman spectrum for a 90 cycles MoS_2 layer. c) AFM topography of an etched area. d) Four-probe sheet resistance for different number of cycles and temperature.

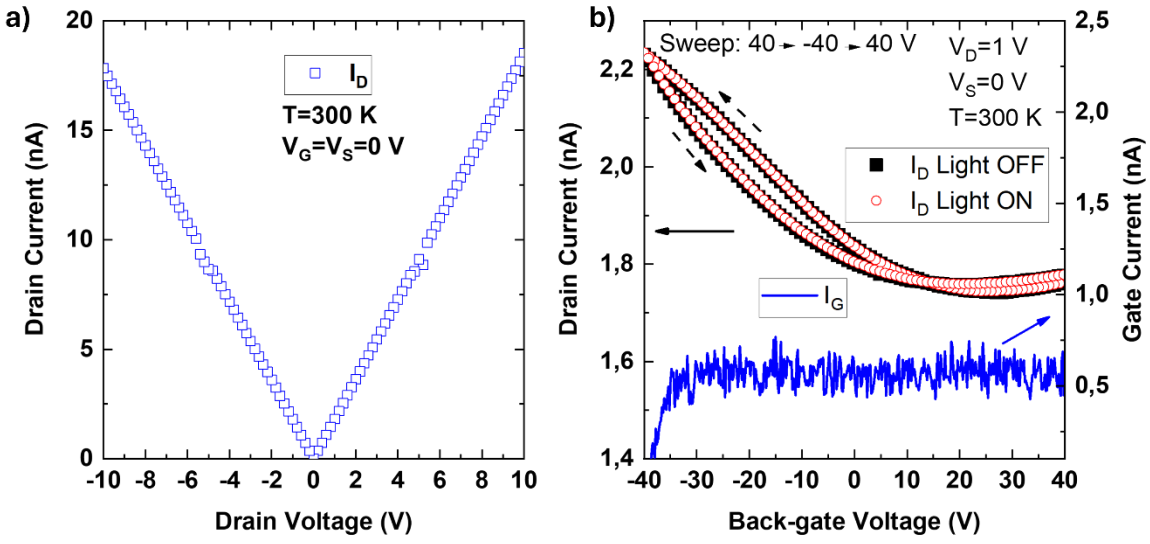

Figure 2: Output a) and transfer b) characteristics for a back-gated MoS_2 device synthesized at 370ºC with 90 ALD cycles. Light corresponds to artificial microscope light conditions. L=45 µm, W=100 µm.