# Trap Characterization in Substrates with Buried SiGe Layers for RF

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When it comes to radio-frequency (RF) applications, an SOI substrate requires low propagation losses and harmonic distortion at microwave frequencies, and this necessitates a high effective resistivity. However, fixed charges present at the BOX/semiconductor bottom interface attract free carriers toward the interface, lowering the effective resistivity of the substrate. This is referred to as the parasitic surface conduction (PSC) that undermines the efficacy of employing a High-Resistivity (HR) substrate. One efficient way to reduce free carriers near the Si surface and conserve the high resistivity of the substrate is to take advantage of a large density of interface traps ($D_{it}$) at the $SiO_2$/Si interface. High interface trapping states lead to deep Fermi level pinning in the band gap, so that the free carrier concentrations remain low, ensuring a state of high resistivity. In our work, an epitaxial SiGe layer is inserted under the BOX between $SiO_2$ and Si. A $SiO_2$/SiGe interface tends to have higher $D_{it}$ values than $SiO_2$/Si, attributed to the formation of Ge-O bonds in the interfacial layer [1]. Consequently, it would be valuable to investigate $D_{it}$ and the effective resistivity ($\rho_{eff}$) in different buried SiGe substrates.

Fig. 1 shows schematic cross-sections of a SiGe MOS capacitor (a) and a coplanar waveguide (CPW) transmission line structure (b). Here, $R_s$ is the series resistance of the Si substrate. $C_{ox}$ is the capacitance of the dielectric stack. $C_c$ and $G_c$ are the corrected capacitance and conductance. $G_p$ and $C_p$ are the parallel equivalent conductance and capacitance, respectively, corresponding to the $SiO_2$/SiGe interface. SiGe/Si is assumed to be interface trap-free. Table I lists the compositions of five buried SiGe substrates and the related thickness of different SiGe.

Using the series resistance correction model (SRC) proposed by Nicollian [2] presented in Fig. 1 (a), Fig. 2 (a) shows $C_c$-$V$ from 1 kHz to 1 MHz. One can see the flatband voltages shift towards negative values with increased frequencies, preventing a conventional flatband extraction. This horizontal frequency-dependent shift can be explained with the effective pinned Fermi level by high $D_{it}$ at the interface $SiO_2$/SiGe [3]. The "bump" arises within the inversion region, where the increase in capacitance under positive bias with decreasing frequency is largely mitigated. This could also be attributed to a high interface trap density effectively stabilizing the Fermi level [4]. The extraction of average substrate p-type doping concentration, $N_A$ ($= 1.10 \times 10^{15}\,cm^{-3}$) is here based on the slope of the linear part of the $(1/C_c)^2$ curve versus the applied voltage in the inset [5], corresponding to 14 Ω·cm for all SiGe samples. Fig.2 (b) shows the $G_p/\omega$ - $f$ curves. The peak positions of the $G_p/\omega$ ($f$) curves shift to high voltage values with decreased frequency due to the presence of interface trap states. Therefore, we obtain the interface trap response for a gate voltage range from -3.5 to 6 V.

Fig. 3 (a) shows the $D_{it}$ ($\Delta E = E_T - E_v$) profiles of samples 3 and 4, the trap energy states distributed in the band from 0.3 to 0.5 eV above the valence band ($D_{it}$ values of all the samples listed in Table I). In Fig. 3 (b), the $\rho_{eff}$ of sample 3 with a higher $D_{it}$ value appears flatter and higher compared to sample 4 in the range of -15 to 15 V. Differing from samples 3 and 4, the $\rho_{eff}$ value of standard Si (15-20 Ω·cm) are lower and dependent on gate bias. The boost of $\rho_{eff}$ is attributed to the higher $D_{it}$ at $SiO_2$/SiGe compared to $SiO_2$/Si. The simulation for sample 3 aligns with its characterization, which can then be used to model high resistivity buried SiGe substrate. To give insight into the potential of SiGe solution in enabling high-quality RF performance, buried SiGe (500 Ω·cm) high resistivity Si substrate (2 kΩ·cm) is employed in the TCAD simulation, as seen in Table I. It presents a high $\rho_{eff}$ above 2 kΩ·cm being bias independent due to the sufficient compensation provided by the interface traps.

Summarizing, the efficiency of the buried SiGe substrate has been characterized. Both small signal measurements and simulations demonstrated that high $D_{it}$ extracted from the conductance method at an $SiO_2$/SiGe interface can neutralize the free carriers coming from bulk, thus overcoming the PSC effect and ensuring a state of high resistivity. High resistivity buried SiGe substrate emerges as a promising candidate for RF SOI integration. At the same time, a buried SiGe layer can be a useful layer being able to induce tensile strain in the channel of an SOI MOSFET if both the SOI and BOX layers are extremely thin (FD-SOI), thereby boosting transistor mobility [6].

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**References:**
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TABLE I SUMMARY OF PARAMETERS OF SUBSTRATES

| Sample number | SiGe thickness (Å) | %Ge | $D_{it}$ ($eV^{-1}cm^{-2}$) | $\rho_{eff}$ (Ω·cm) @ 2 GHz @ 0 V |
|---|---|---|---|---|
| **1** | 90 | 20 | $2.2 \times 10^{12}$ | 44.6 |
| **2** | 130 | 20 | $2.2 \times 10^{12}$ | 44.8 |
| **3** | 700 | 20 | $2.5 \times 10^{12}$ | 44.8 |
| **4** | 60 | 40 | $1.8 \times 10^{12}$ | 40.6 |
| **5** | 110 | 30 | $8.0 \times 10^{11}$ | 41.5 |
| **Standard Si** | - | - | $2.5 \times 10^{11}$ [2] | 21.5 |
| **500 Ωcm SiGe/HR Si (TCAD)** | 1100 | 20 | $2.2 \times 10^{12}$ | 5213 |

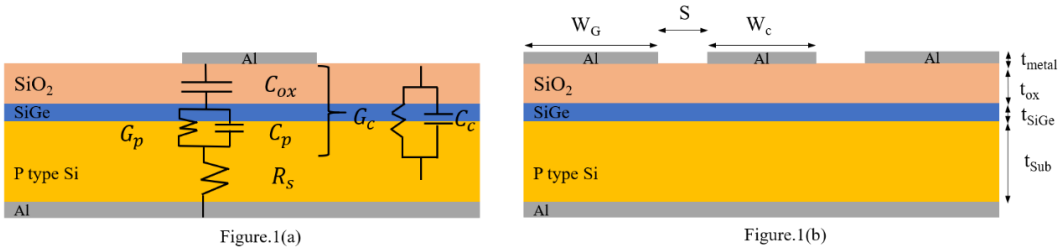


Figure 1. (a) The cross-section of SiGe buried capacitor. (b) The cross-section of a CPW line on top of SiGe buried substrate (Parameters: $t_{metal}$ = 1 um, $t_{ox}$ = 200 nm, $W_c$ = 26 µm, $W_G$ = 208 µm, and $S$ = 12 µm).

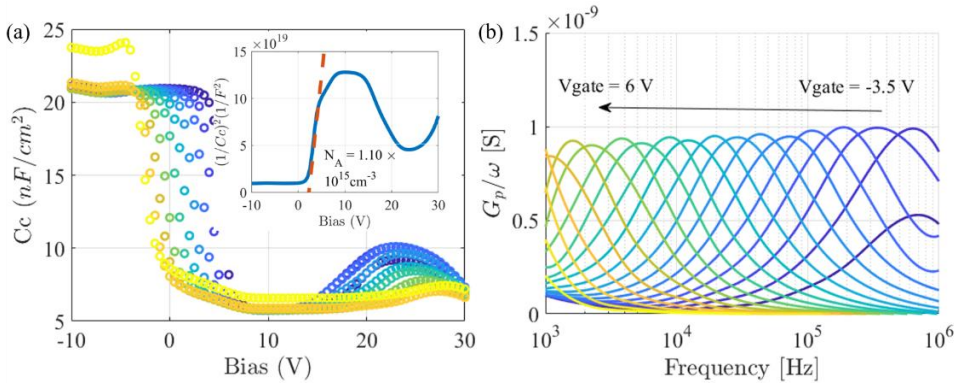


Figure 2. (a) $C_c$ – $V$ and (b) $G_p/\omega$ - $f$ from 1 kHz to 1 MHz for sample 2. The inset in (a) corresponds to $N_A$ extraction.

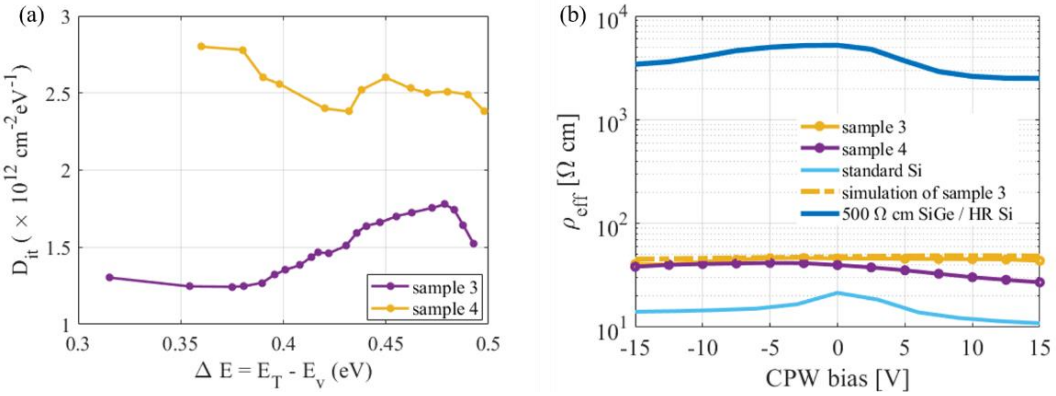


Figure 3. (a) $D_{it}$ ($\Delta E = E_T - E_v$) profile of samples 3 and 4, respectively. (b) CPW line effective resistivity of samples 3, 4, standard Si, and 500 Ω cm SiGe/HR Si extracted at 2 GHz as a function of applied bias from -15 to 15 V.