Analysis of Electron Mobility in 7-Level Stacked Nanosheet GAA nMOSFETs

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Gate-all-around (GAA) nanosheet (NS) transistors have been proposed and demonstrated to be a competitive alternative to FinFETs, aiming to increase current drivability by footprint [1, 2], required to push the scaling limits of CMOS technology. The fabrication of GAA NS transistors with 7 stacked channels has been successfully presented, showing significant improvements compared to 2 levels [3]. It is well-known that in multiple-gate MOSFETs, current flows in different crystallographic planes, the orientation being (100) and (110) at the top/bottom and sidewalls, respectively, resulting in different mobility values. Therefore, this work details transport parameters of n-type 7-level stacked nanosheet GAA MOSFETs. The contributions of horizontal and sidewalls to mobility and degradation factors are analyzed separately in NS with several channel lengths.

The GAA Stacked NS nMOSFETs measured in this work were fabricated at CEA-Leti according to the process described in [3]. Fig. 1 shows a TEM and EDS spectroscopy of GAA NS transistors with 7 stacked channels [3]. The experimental mean drain current (I_D) as a function of gate voltage (V_G), and the transconductance (g_m) measured with a drain bias of V_{DS}= 25mV for NS with width W_{NS} = 15nm and 55 nm and different channel lengths (L) are presented in Fig. 2 and 3, respectively. The results clearly show that the subthreshold slope (SS) is close to the theoretical limit even for the device with L = 50 nm and W_{NS} = 55 nm, which presents SS = 60.5 mV/dec, showing excellent electrostatic control. Aiming to separate the contribution of horizontal (top and bottom channels) and vertical (sidewalls) conduction planes, the drain current has been plotted as a function of the nanosheet width for different values of V_G, with the sidewalls current ($I_{D,side}$) obtained at W_{NS} = 0 [4]. The current on the 13 horizontal conduction planes ($I_{D,top}$) is then calculated as the difference between I_D and $I_{D,side}$. The top and sidewalls components of I_D and g_m for the devices with L = 100 nm and different W_{NS} are presented in Fig. 4. As the NS is narrowed, approaching the silicon film height (H_{NS}), the contribution of the sidewalls in the total I_D becomes of the same order of magnitude than the horizontal planes. The threshold voltage (V_{TH}), low-field mobility (μ_0), and its degradation factors were extracted from these curves using the Y-Function methodology. As shown in Fig. 5, the V_{TH} of the sidewalls is slightly larger than at the top, which is responsible for fixing the overall V_{TH} of the devices, independent of L or W_{NS}. From the results shown in Fig. 6, one can note that, unlike observed for FinFETs, the sidewall mobility is not reduced compared to that in the horizontal conduction planes. The linear and quadratic mobility degradation factors, θ_1 and θ_2, are presented in Figs. 7 and 8, respectively. The extracted results for θ_1 (related to phonon and Coulomb scattering) and θ_2 (related to surface roughness), show that both degradation factors are larger at the horizontal surfaces than at the sidewalls regardless of L. Negligible θ_1 is observed at the sidewalls, which contributes to reducing the overall θ_1 in narrow NS. On the contrary, θ_2 has been shown to increase as the NS is narrowed.

References

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[4] K. Bennamane, et al., Solid-State Electronics, 53, p. 1263 (2009).

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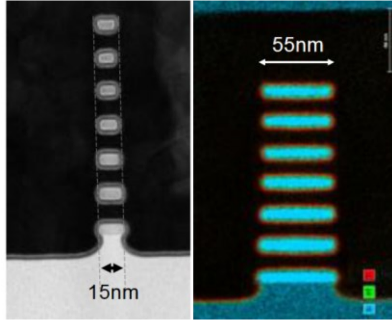

Fig. 1. TEM and EDS spectroscopy of GAA NS transistors with 7 stacked channels [3].

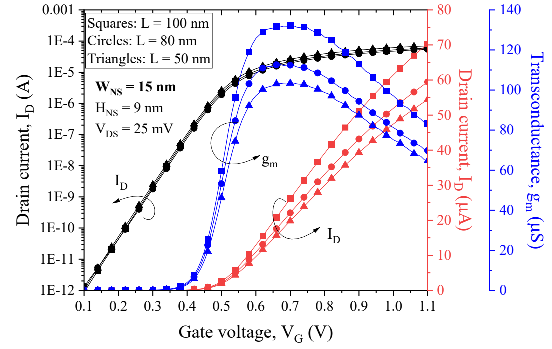

Fig. 2. Experimental mean drain current and transconductance as a function of the gate voltage, for GAA stacked NS with W_{NS} = 15 nm and different L.

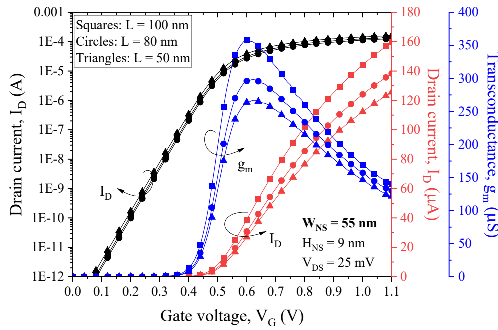

Fig. 3. Experimental mean drain current and transconductance as a function of the gate voltage, for GAA stacked NS with W_{NS} = 55 nm and different L.

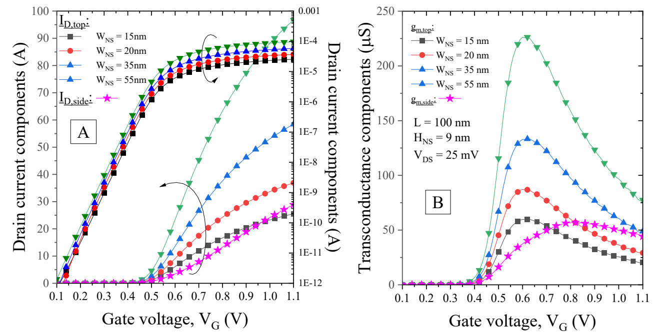

Fig. 4. Top/bottom and sidewalls components of I_D (A) and g_m (B) as a function of the gate voltage for stacked GAA NS transistors with L = 100 nm and different NS widths. All curves measured with V_{DS}= 25mV.

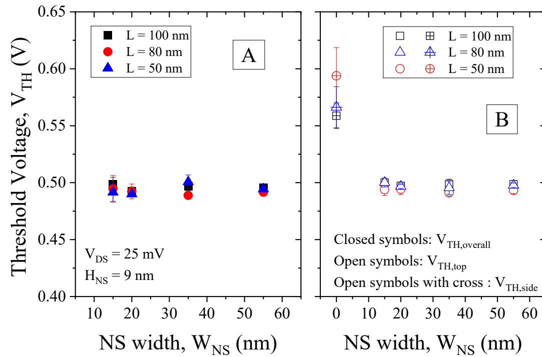

Fig. 5. Total, top and sidewall threshold voltage *vs* W_{NS} for GAA stacked NS with different channel lengths.

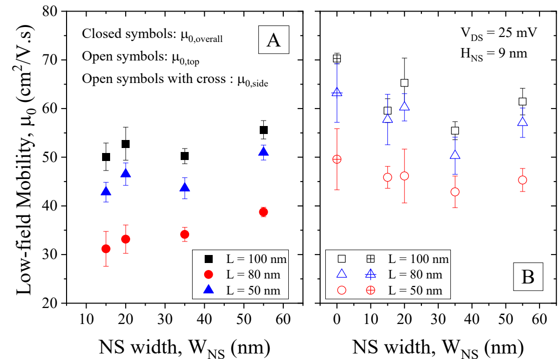

Fig. 6. Total, top and sidewall low-field mobility *vs* W_{NS} for GAA stacked NS with different lengths.

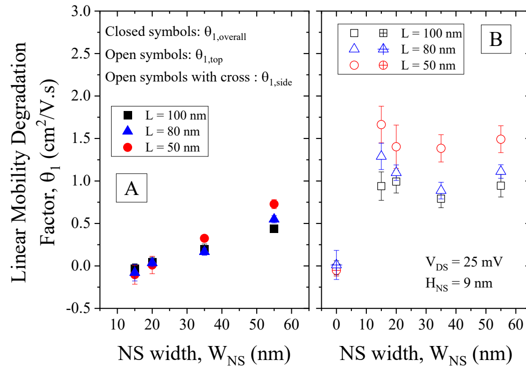

Fig. 7. Total, top and sidewall linear mobility degradation factor *vs* W_{NS} for GAA stacked NS with different channel lengths.

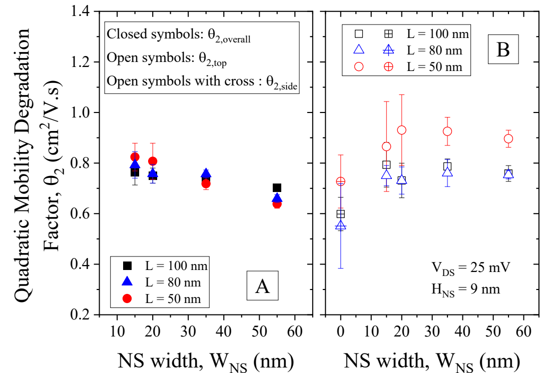

Fig. 8. Total, top and sidewall quadratic mobility degradation factor *vs* W_{NS} for GAA stacked NS with different channel lengths.