Experimental Extraction of Self-Heating in SOI Nanowire MOSFETs at Cryogenic Temperatures

F. E. Bergamaschi[1], J. A. Matos[2], J. C. Rodrigues[2], G. A. Matos[2], S. Barraud[1], M. Cassé[1],

O. Faynot[1], M. A. Pavanello[2*]

[1]*CEA-Leti, Université Grenoble Alpes, F-38000 Grenoble, France*

[2]*Department of Electrical Engineering, Centro Universitário FEI, São Bernardo do Campo, Brazil*

The self-heating effect (SHE) is a notorious challenge when it comes to CMOS performance, particularly in the context of Silicon-On-Insulator (SOI) MOSFETs [1]. This phenomenon consists of the temperature increase in the conduction channel due to the heat flow generated by the drain current in addition to the difficulty of dissipating that heat, which is related to the high thermal resistance of the buried oxide of SOI devices. Furthermore, it is known that SHE is intensified in cryogenic environments [2], which is of major importance for specific applications such as quantum computing [3]. This work aims to demonstrate the experimental results of SHE in fully depleted (FD) Ω-gate SOI Nanowire MOSFETs obtained using the gate resistance thermometry technique in a wide temperature range from 300K down to 4.2K.

Fig. 1 presents a 3D schematic of an SOI nanowire with the two-contact gate structure, necessary for the self-heating extraction technique. The devices were fabricated at CEA-Leti following the process of [4]. Fig. 2 shows the measured drain current (I_{DS}) as a function of the gate voltage (V_{GS}) for nanowires with L of 100nm and 40nm for ambient temperatures (T_{AMB}) from 300K down to 4.2K. The Zero Temperature Coefficient (ZTC) points demonstrate negligible series resistance in the whole temperature range. Fig. 3 presents the calibration of the electrical resistance of the metal gate (R_{GATE}), measured between the contacts Gate 1 and Gate 2, as a function of the ambient temperature (T_{AMB}) with the device in off-state. For the nanowire with L=100nm, in the linear region R_{GATE} increases with T_{AMB} at a rate of 0.37 Ω/K, while for L=40nm, the rate is 0.21 Ω/K. The variation of R_{GATE} with T_{AMB} is considerably smaller than that reported for planar FDSOI transistors in [5], which have a rate of 2.12 Ω/K. A saturation of R_{GATE} is observed for T below 20K, also demonstrated in [5]. Using the calibration curves from Fig. 3 and the I_{DS}-V_{GS} curves from Fig. 2, it was possible to extract the channel temperature increase (ΔT) as a function of the dissipated power ($P=V_{DS} \times I_{DS}$), with the results presented in Fig. 4. The increase of ΔT with the reduction of T_{AMB} demonstrates the stronger self-heating at lower temperatures. For $T_{AMB} \geq 50K$, the ΔT curves are roughly linear in the whole range of P. In contrast, below this temperature, the temperature increase presents a non-linear dependency with the power, where a steeper raise of ΔT is observed at the low power region, below 5μW. Fig. 5 compares the temperature increase between both channel lengths (100nm and 40nm) at same ambient temperatures, of 100K and 300K, indicating a higher ΔT for shorter devices: for a fixed power of 35μW, at T_{AMB}=100K the temperature increase is approximately 17K for L=40nm, while the nanowire with L=100nm heats up around 11K. Fig. 6 presents the differential thermal resistance (R_{TH}*), calculated as the derivative of the ΔT *vs.* P curves, as a function of the device temperature ($T_{DEV}=T_{AMB}+\Delta T$). The thermal resistance sharply increases below 70K, while a weaker dependency with the temperature is observed at higher T_{DEV}. This tendency agrees with the results of [6] for planar FDSOI transistors, although the R_{TH}* values are significantly higher for the nanowires, due to the thicker buried oxide layer (145nm, against 25nm of the planar device) and the highly confined active silicon region, both which hinder the heat diffusion.

* Corresponding author: Marcelo Antonio Pavanello email: pavanello@fei.edu.br

References

[1] B. M. Tenbroek et al, IEEE Trans. Electron Devices, vol. 43, no 12, p. 2240–2248, 1996

[2] A. A. Artanov et al., IEEE Trans. Electron Devices, vol. 69, no 3, p. 900–904, 2022.

[3] B. Patra et al., IEEE J. Solid-State Circuits, vol. 53, no 1, p. 309–321, 2018.

[4] S. Barraud et al., IEEE Electron Device Lett., vol. 33, no 11, p. 1526–1528, 2012.

[5] K. Triantopoulos et al., IEEE Trans. Electron Devices, vol. 66, no 8, p. 3498–3505, 2019.

[6] M. Cassé et al., 2022 International Electron Devices Meeting, p. 34.6.1-34.6.4, San Francisco, Dec. 2022.

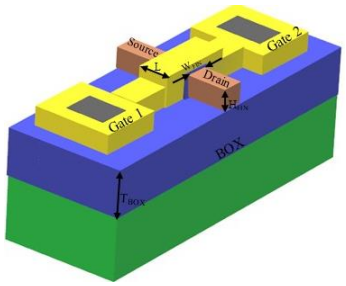

Figure 1 – 3D schematic of a nanowire with the 2-contact gate structure indicating the main geometrical parameters.

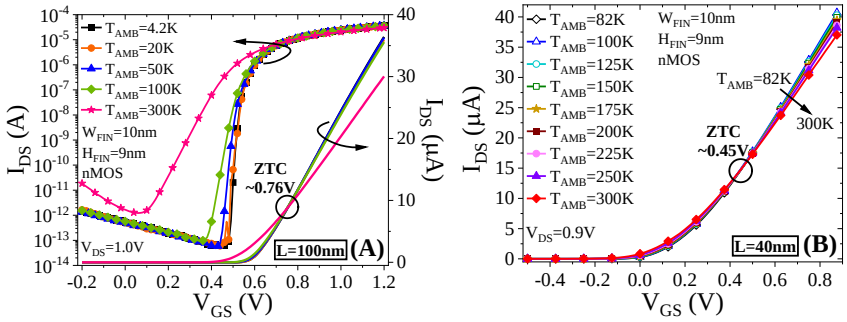

Figure 2 – Measured drain current as a function of the gate voltage for nanowires with (A) L=100nm and (B) L=40nm, both with W_{FIN}=10nm and H_{FIN}=10nm, at different ambient temperatures.

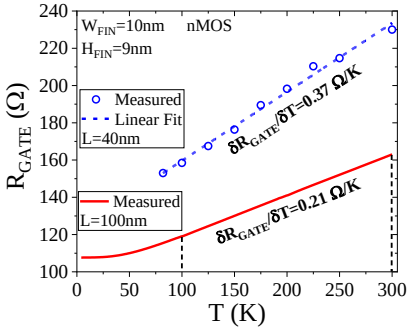

Figure 3 – Gate resistance as a function of the temperature for nanowires with L of 100nm and 40nm in off-state.

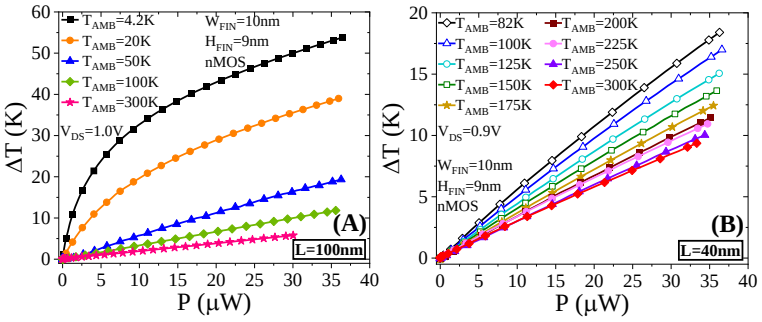

Figure 4 – Channel temperature increase as a function of the dissipated power for nanowires with (A) L=100nm and (B) L=40nm at different ambient temperatures.

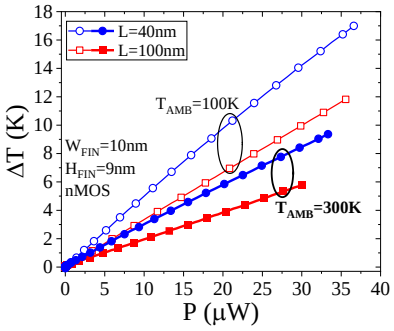

Figure 5 – Comparison of the channel temperature increase for nanowires with L of 100nm and 40nm at T_{AMB} of 100K and 300K.

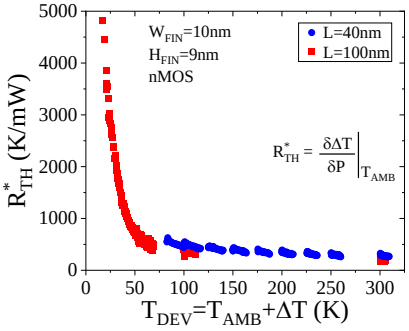

Figure 6 – Differential thermal Resistance as a function of the device temperature for nanowires with L of 100nm and 40nm.