Low-Loss Silicon Substrates with PN Passivation in 28 nm FD-SOI

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In RFICs signals propagate in metals atop insulator-semiconductor stacks, such as in a coplanar waveguide (CPW) is depicted in Fig. 1a. To avoid losses in such lines and coupling between them, the underlying substrate should present high *effective resistivity*. This is achievable using high-resistivity (HR) handle silicon, but beyond that, special passivation must be made at the Si/dielectric interface to avoid the formation of a highly conductive layer (inversion or accumulation). Such *parasitic surface conduction* can be countered using an interface rich in traps, though such solutions are incompatible with FD-SOI. This paper presents an alternative solution using PN junctions [1,2] applied to STMicroelectronics' 28 nm FD-SOI, run on HR substrates for the first time.

The principle behind the PN passivation is to interrupt the interface conduction layer with highly resistive depletion regions that are induced at alternating PN boundaries [1]. Fig. 2 plots the resistivity profile along the Si interface, highlighting the high-resistivity peaks at the PN junctions that dominate the value of the effective interface sheet resistivity. That sheet resistivity is higher-valued the larger the PN junction density per unit of distance along the interface. A depletion density can be defined as the ratio of W_{dep} over the pitch P (see Fig. 2). To maximize the depletion density, large values of W_{dep} and low values of P are sought [1,3]. W_{dep} is set by implant conditions, and lower-ranged doses are then preferred to maximize it [1]. Low values of P are achieved using the tightest lithography available in the process for substrate implants. However, using the most aggressive pitch can lead to undesired electrical coupling and connections between different wells. This problem is highlighted in Fig. 1c: if the depths of the N and P implants are not well balanced, using a tight-pitch results in connection between the deeper polarity wells via the region below the shallower wells. Fig. 1d shows that even if that same depth-imbalance exists while using larger pitch values, the problem is avoided.

Aiming for the best possible results using the tightest pitch values, 10 different wafers were processed with variations in the implant conditions attempting to achieve an optimal depth-implant balance suitable for the most aggressive pitch parameter. Fig. 3 plots the effective resistivity and line losses extracted [4] from the measured CPW lines (cross section and dimensions given in Fig. 3b for two types of CPWs) for select wafers. The results demonstrate for the M1LB lines that the 30 GHz losses can be reduced from 2.75 to 1.06 dB/mm using a high resistivity (around 1 kΩcm) substrate over the standard 10 Ωcm one, and that the loss can be further reduced down to 0.36 dB/mm when using the PN passivation (W09). Similar observations can be made for the IBLB lines (see Fig. 3c).

Table I and Table II recap the extracted effective resistivity and line loss values on all 10 wafer splits for the M1LB lines. Samples from Table I employ normalized P and N implant doses of 100%, while samples in Table II employ halved doses. The splits are made in N and P implant energies, to try and achieve ideal depth balance between neighbouring wells. The implant parameters pertaining to wafers W01, W02, W08, W04, W05 and W10 are imbalanced, with the N wells being deeper than the P wells, and parasitic N-well to N-well coupling happening in those wafers, bypassing the resistive depletion region at the interface, as depicted in Fig. 1c. Thanks to the split wafer processes, wafers W03, W07, W06 and W09 achieve good balance and high performance RF results by implanting the N wells shallower with reduced energy or by implanting the P wells deeper with higher energy. In those cases, effective resistivities up to 540 Ωcm can be achieved, with losses reduced to 0.36 dB/mm.

Experiments on the same 10 wafers utilising relaxed-pitch PN implant patterns below the same lines were run. When the PN pitch is relaxed to 2x the minimum value, all wafers achieve ρ_{eff} values in the range of 250 to 350 Ωcm. Since the depletion density is reduced (see Fig. 2), values of 400 to 540 Ωcm are no longer attainable, but the passivation becomes more robust to the implant conditions, since with that relaxed pitch, all 10 different implant parameters yield decent (~300 Ωcm) results.

Overall, this work demonstrates excellent RF substrate loss reductions in 28 nm FD-SOI.

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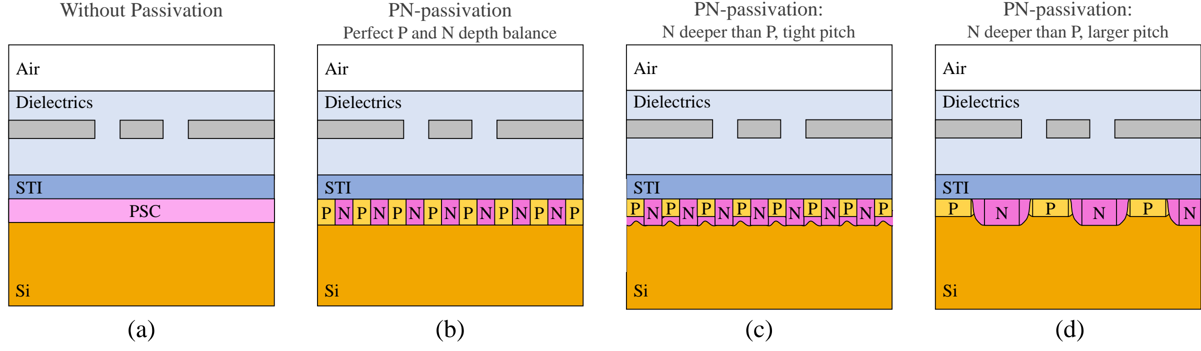

Fig. 1: CPW above (a) an unpassivated substrate with PSC (a), and above three types of PN-passivated substrates (b), (c) and (d).

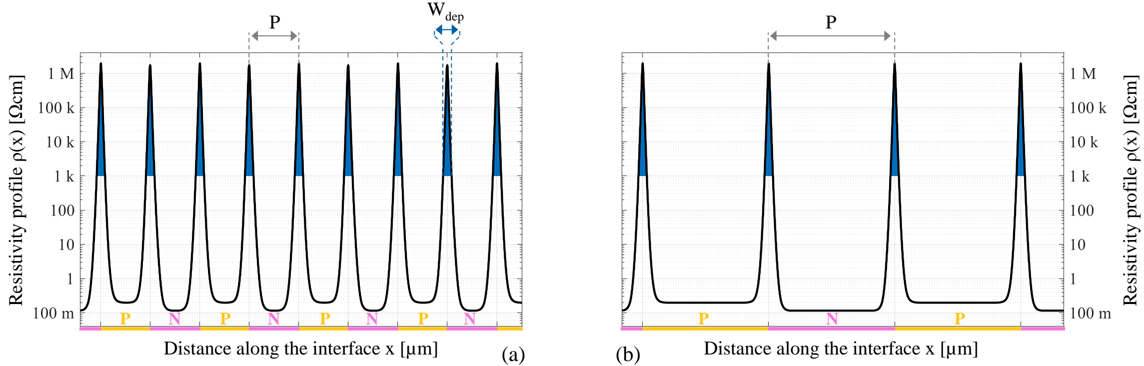

Fig. 2: Local resistivity profile ρ(x) along the Si/STI interface passivated with alternating PN junctions (obtained from TCAD simulations prior to wafer processing). (a) using a tight pitch achieving a depletion ratio of W_{dep}/P = 20%, and (b) using a relaxed pitch achieving 7%.

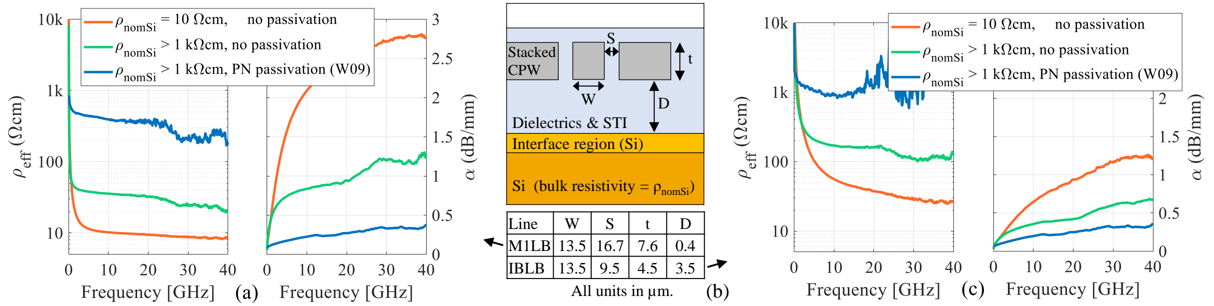

Fig. 3: Effective resistivity and line loss extracted from M1LB (a) and IBLB (c) lines for selected wafers. (b) Geometry of the CPW lines.

Wafer ID	Energy P [%]	Energy N [%]	ρ_{eff} [Ωcm]	Line loss at 30 GHz [dB/mm]	Comment
W01	100	100	76	0.67	N too deep relative to P
W02	90	100	45	0.94	N too deep relative to P
W03	**110**	100	400	0.41	Good balance with **deeper P**
W07	100	**90**	400	0.42	Good balance with **shallower N**
W08	100	110	25	1.26	N too deep relative to P

Table I: RF Performance from M1LB CPW Lines of Wafer Splits in PN Implant Energy for Doses of 100%.

Wafer ID	Energy P [%]	Energy N [%]	ρ_{eff} [Ωcm]	Line loss at 30 GHz [dB/mm]	Comment
W04	100	100	200	0.44	N too deep relative to P
W05	90	100	150	0.50	N too deep relative to P
W06	**110**	100	500	0.37	Good balance with **deeper P**
W09	100	**90**	540	0.36	Good balance with **shallower N**
W10	100	110	61	0.72	N too deep relative to P

Table II: RF Performance from M1LB CPW Lines of Wafer Splits in PN Implant Energy for Doses of 50%.

References

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