Thermal-coupling characterization of FD-SOI FETs at cryogenic temperatures

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Quantum computers have the potential to solve problems computationally unfeasible on classical computers [1]. For proper operation, the qubits need to be cooled down to cryogenic temperatures with its control electronics placed in close vicinity. However, self-heating can raise the device temperature significantly above the ambient temperature and its surroundings [2,3], which degrades device performance and can also alter qubit state.

This work studies thermal cross-coupling between two side-by-side FD-SOI MOSFETs at liquid nitrogen temperatures in comparison to the room temperature one. We demonstrate that electrical parameters degradation caused by the operation (heating) of the neighbor device can be up to 50 % more important at 77K than at 295K.

Devices under study: The devices under study are fabricated by an industrial FD-SOI process. They consist of two multi-fingers nFETs placed side-by-side at 2.76 µm distance from each other (Fig. 1): (i) FET 1 features a gate length (L) < 30 nm and a total width (W) of 8 µm and (ii) FET 2 (heater) features L < 30 nm W of 32 µm.

Experimental results and discussion: Fig. 2 shows I_d-V_{gs} characteristics of FET 1 biased in a linear regime and different temperatures, highlighting a strong temperature dependence, particularly in the subthreshold region. The corresponding variations of g_m/I_d of FET 1 (Fig. 3) serve as a temperature calibration to estimate afterwards the temperature rise in FET 1 when FET 2 operates and its heat propagate to the surroundings. Fig. 4 plots I_d-V_{gs} curves of FET 1 biased in a linear regime when FET 2 is biased in cold FET mode ($V_2 = V_{gs2} = V_{ds2} = 0$ V) and in different operation conditions in saturation and strong inversion regimes (V_2 = 0.5, 0.6, 0.8 and 0.9 V) at both 77 K and 295 K. A linear reduction of g_m/I_d of FET 1 vs the power of FET 2 from 85.5 (31.1) to 74.6 (29.3) V^{-1} at 77 K (295 K) is highlighted in Fig. 5. By using g_m/I_d of FET 1 vs temperature plot (Fig. 3), one can estimate a temperature increase of ΔT = 46 K and 4 K at 77 and 295 K, respectively, demonstrating strong sensibility to thermal coupling (TC) effects at cryogenic temperature. Keeping this in mind, the following part of this work is focused on the analysis TC effect on various figures of merit (FoM) of FET 1, i.e. when it is operating in saturation regime. One of the main FoM for digital applications is the I_{on}/I_{off} ratio. While I_{off} is classically measured at $V_{gs} = 0$ V, I_d in this conditions becomes very small (< 10^{-10} A) at 77 K, so it is decided to take I_{off} at V_{gs} = 0.1 V in the framework of this work, so that $I_{on} = I_d(V_{gs} = V_{ds} = 0.8$ V) and $I_{off} = I_d(V_{gs} = 0.1$ V, $V_{ds} = 0.8$ V). As shown in Fig. 6, I_{on}/I_{off} ratio suffers a significant 77 % reduction at 77 K when FET 2 is biased at V_2 = 0.9 V while this reduction is limited to 25 % at 295 K. This degradation of the I_{on}/I_{off} ratio is strongly related to the increase of I_{off} (Table 1). Another FoM, particularly important for analog applications, is the transconductance (here extracted as peak value at V_{ds} = 800 mV), which appears only slightly degraded by the operation of FET 2 with a reduction of 1.7 % (1.5 %) at 77 K (295 K) (Table 1). Indeed, in saturation and inversion regimes FET 1 itself is subjected to self-heating making it less sensitive to external heat sources (e.g. cross-thermal coupling). In weak inversion regime (at V_{ds} = 800 mV) at $I_d = 10^{-7}$ A, g_m/I_d decreases with V_2 from 69.6 to 63 V^{-1} (-9.5 %) at 77 K and from 30.2 to 29.2 (-3.3 %) at 295 K (Table 1).

Conclusion: The impact of TC (and related temperature rise) was demonstrated on different FoM. Temperature rise in FET1 due to operation of FET 2 was revealed to be stronger at 77 K (ΔT = 46 K) wrt 295 K (ΔT = 4 K). FoMs degradation is more important at 77 K than 295 K with a maximum of 77% reduction of I_{on}/I_{off} at 77 K wrt 25 % at 295 K when the neighbor device is biased at 0.9 V due to stronger temperature increase at 77 K.

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References

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[3] P. A. T Hart *et al.*, *IEEE Journal of the Electron Devices Society*, vol. 9, pp. 891–901, 2021.

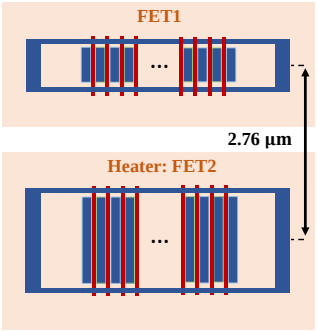

Fig. 1. Schematic (not to scale) of two multi-fingers FD-SOI nFETs placed 2.76 µm away from each other. Bottom FET is used to heat the top FET.

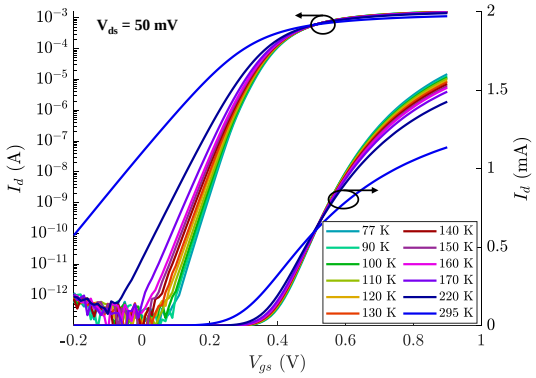

Fig. 2. Drain current I_d of FET 1 vs gate voltage V_{gs} in linear regime (V_{ds} = 50 mV) at different temperatures.

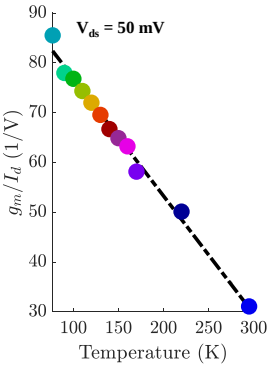

Fig. 3. g_m/I_d of FET 1 extracted at $I_d = 10^{-9}$ A vs temperature in linear regime (V_{ds} = 50 mV).

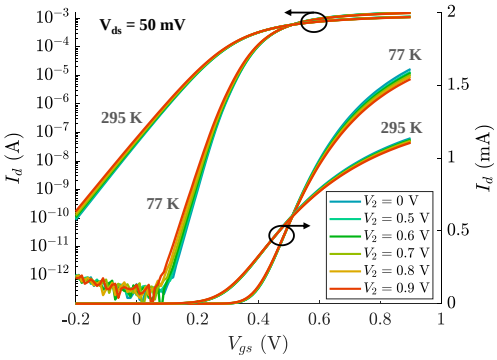

Fig. 4. I_d of FET 1 vs gate voltage V_{gs} in linear regime (V_{ds} = 50 mV) at 77 K and 295 K when FET 2 is under different bias conditions.

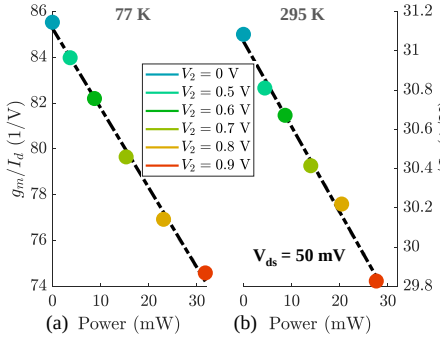

Fig. 5. g_m/I_d of FET 1 vs dissipated power of FET 2 at 77 K and 295 K, when FET 1 is biased at V_{ds} = 50 mV.

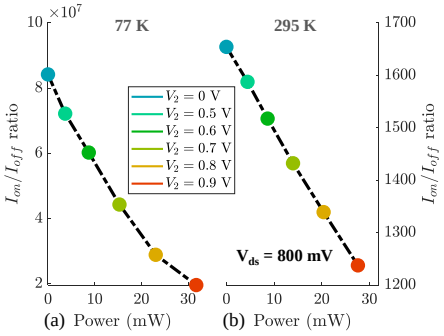

Fig. 6. I_{on}/I_{off} ratio of FET 1 vs dissipated power of FET 2 at 77 and 295 K, when FET 1 is biased at V_{ds} = 800 mV. I_{on} and I_{off} are respectively defined at V_{gs} of 0.8 and 0.1 V).

TABLE I. THERMAL-COUPLING IMPACT ON DIFFERENT FOM IN LINEAR (GREEN) AND SATURATION (BLUE) REGIMES.

FoM	Temperature (K)	V_2 = 0 V	V_2 = 0.9 V	FoM(V_2 = 0.9 V) vs FoM(V_2 = 0 V)
SS (mV/dec)	77	26.9	30.9	+ 14.9 %
	295	74.1	77.2	+ 4.2 %
V_{th} (V)	77	0.392	0.387	ΔV_{th} = - 0.005 V
	295	0.296	0.288	ΔV_{th} = - 0.008 V
I_{off} (A)	77	0.85×10^{-10}	3.60×10^{-10}	+ 323 %
	295	3.79×10^{-6}	5.03×10^{-6}	+ 32.7 %
I_{on}/I_{off}	77	84.2×10^{6}	19.6×10^{6}	- 76.7 %
	295	1.65×10^{3}	1.24×10^{3}	- 24.8 %
g_m (mS)	77	17.87	17.56	- 1.7 %
	295	13.58	13.37	- 1.5 %
g_m/I_d (1/V) @ $I_d = 10^{-7}$ A	77	69.6	63.0	- 9.5 %
	295	30.2	29.2	- 3.3 %