Engineering Thin HZO Ferroelectric Layers: From Material Study to 3D Integration for Vertical Gate-All-Around FeFETs

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The demand for higher computational efficiency and lower energy consumption in semiconductor devices has led to the exploration of non-traditional computing architectures. One promising direction is the integration of logic and memory into a single device or cell, potentially overcoming the limitations of the Von Neumann architecture. This paradigm is now within reach thanks to the introduction of CMOS compatible ferroelectric materials, such as hafnium oxide (HfO_2), known for its reversible residual polarization under the effect of external electric fields[1].

This study presents a thorough investigation of the Hf-Zr ($Hf_{0.5}Zr_{0.5}O_2$ - HZO) layer and the subsequent steps towards its integration into 3D gate-all-around devices [2], currently targeted for the next technology nodes in logic architecture. Fig.1 shows planar MIS devices, with a 10nm HZO layer, that display through GIXRD the successful crystallization of HZO with annealing temperatures starting as low as 400°C. The ferroelectricity and thus the orthorhombic crystalline phase of HZO is verified through pulsed electrical measurements which exhibit a robust (P-E) hysteresis loop. Integration on vertical nanostructured channels has been successfully demonstrated (Fig. 2) with a perfect conformity of the layer. In a 3D nanoscale configuration, identifying the proper ferroelectric phase with classical approaches (such as GIXRD) used in planar structures is not feasible. So, we developed a novel approach that couples 4DSTEM imaging and python based data processing to perform a full mapping of the grains and crystalline phases of our HZO layer.

Furthermore, we investigate the challenges related to integrating the HZO layer into 3D nanostructures, particularly selective and anisotropic etching steps, to maintain the integrity of the HZO layer (see Fig. 2). This ensures the removal of unwanted layers from our nanostructures while preserving the surrounding HZO layer, facilitating the subsequent formation of alloy contacts. Additionally, considering the opportunities and possible limitations of fabrication parameters, we explore different process routes in parallel (S/D contact first/last) for the 3D integration of HZO in gate all-around FeFETs (see Fig. 3), discussing the pros and cons of each configuration (metallurgy stability of the contacts, doping segregation at the interfaces etc).

References

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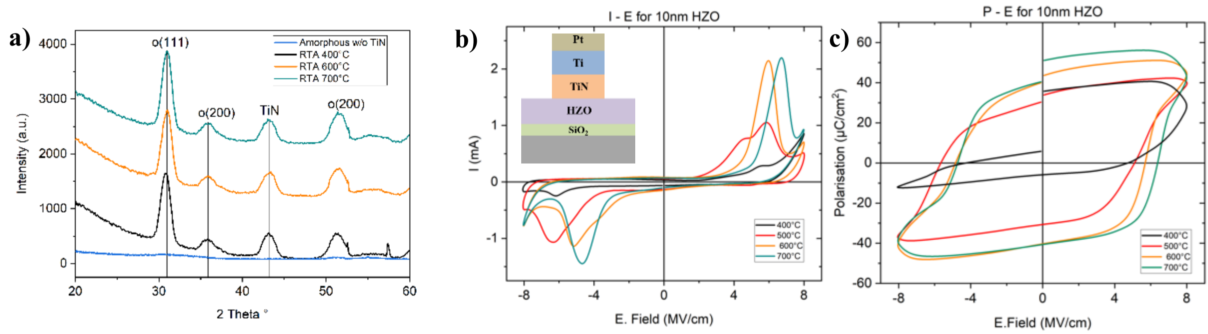

Figure 1: (a) GIXRD verification of the crystalline nature and identification of the orthorhombic phase on our planar samples. The electrical measurements were conducted on a stack of 1.5nm of SiO_2 on Si substrate followed by 10nm of HZO, 13nm of TiN and a total of 35 nm of Ti/Pt as top contact. Results of I vs E_{field} (b) and P vs E_{field} (c) demonstrate the evolution of polarization and Ec for different HZO activation annealing temperatures.

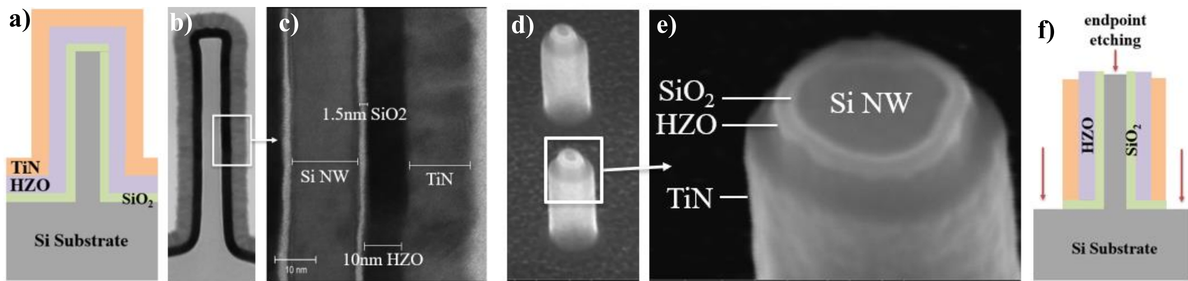

Figure 2 : (a)Schematic of the vertical HZO/TiN deposition. (b) TEM from vertical nanowire with crystalized SiO2/HZO/TiN multistack with a (c) zoomed view on the critical sidewall. (d)birds view SEM plasma etched vertical nanowires where TiN/HZO have been removed from (e) top and bottom with the corresponding 2D sketch(f)

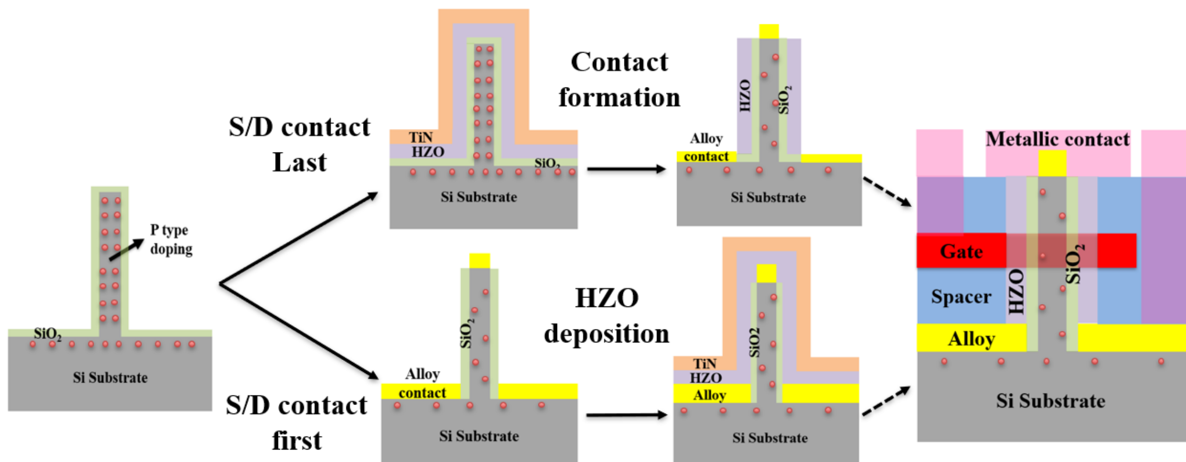

Figure 3 : The two different fabrication approaches process flow of a Vertical Nanowire GAA FeFET (S/D contact first/last). The red dotes demonstrate the p type doping. The stabilization and integrity of the formation of the alloy contact is critical in order to ensure good electrical properties of the transistor.

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