Effect of Al_2O_3 on the operation of SiN_X-based MIS RRAMs

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A large variety of resistive memory (RRAM) technologies are prominent. Nevertheless, a few fulfill the requirements for CMOS integration and meet the commercialization standards. SiN_X was found to exhibit competitive resistance switching (RS) properties and attractive SiN_X-based RRAM devices have been recently demonstrated [1-3] utilizing a metal-insulator-semiconductor structure comprising 7nm LPCVD SiN_X (x = 1.27) on heavily doped n^{++} Si ($N_d = 1\times10^{20}$ /cm^3) and 30nm Cu acting as bottom (BE) and top electrode (TE) respectively. Al_2O_3 has been used in the past as a buffer layer in RRAMs to improve the RS and the cycle-to-cycle variations [4]. In this context, we investigated the effect of inserting a thin Alumina layer between the top electrode and SiN. A reference sample without the Al_2O_3 was prepared for the shake of comparison (Figure 1). The 3nm Al_2O_3 layer was deposited by MEMS ALD. The TE was covered by a 30nm Pt to prevent oxidation.

Figure 2a presents I-V curves measured for different compliance currents (I_{CC}). The SET and RESET voltages were statistically analyzed in Figure 2b and statistical analyses revealed that the addition of Al_2O_3 slightly reduced the HRS variability. Nevertheless, LRS variability increased. The mean SET voltage of the Al_2O_3/SiN_X sample is 0.9V higher than the reference, which equals the voltage drop on the Al_2O_3 when 5V is applied to the TE according to simulation results. This means that the addition of Al_2O_3 on SiN_X does not alter its operation as a switching material. Multiple SET/RESET cycles were performed using voltage sweeps (I_{CC} 100μA). The current at high resistance (HRS) and low resistance (LRS) states is monitored at 0.5V. The Al_2O_3/SiN_X can endure significantly lower number of cycles compared to the reference sample which is probably be attributed to the higher SET/RESET voltages used for Al_2O_3/SiN_X sample. The memory window (LRS/HRS) evolution with the number of cycling voltage is shown in Figure 2c. Specifically, it begins at 10^4 and is stabilized to 10^5. This behavior has been previously observed in reference samples [6] and is attributed to the gradual reduction of the length of the raptured conductive filaments during cycling.

Moreover, impedance spectroscopy measurements were performed for pristine and cycled devices, i.e., after the SET/RESET sweeps using different SET I_{CC}. The Nyquist plots for Al_2O_3/SiN_X devices at LRS form a semicircle (Figure 3a), indicative of an equivalent circuit consisting of a resistor (R_p) and a capacitor (C_p) in parallel and a resistor in series (R_s). Physically, R_p and C_p correspond to the resistance of the conductive paths formed during SET and the capacitance of the remaining insulating (no-switched) material region, respectively. The dielectric constant (ε') was also extracted (Figure 3b) for pristine samples, and it was found to be significantly higher (~7.7) than the reference sample (~5.5),

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which is expected due to the addition of the 3nm Al_2O_3. Furthermore, the AC conductance (σ') was calculated (Figure 3c) by subtracting the dc part from the measurements and it becomes clear that σ' varies as ~f^s. The values of exponent s range from 1.59 to 1.67 and denote that during SET conduction in SiN_X is mainly governed by trap-to-trap tunneling mechanisms (s is close to 2) [5].

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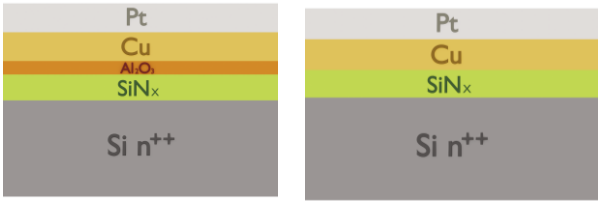

Figure 1 Fabricated Al_2O_3/SiN_X and SiN_X (reference) samples.

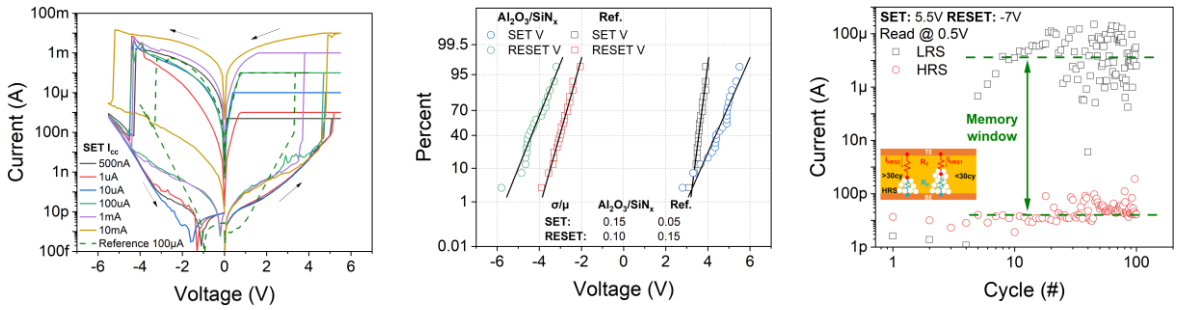

Figure 2 a) I-V sweeps with different I_{CC}, b) SET/RESET voltage statistics and c) HRS/LRS at 0.5V.

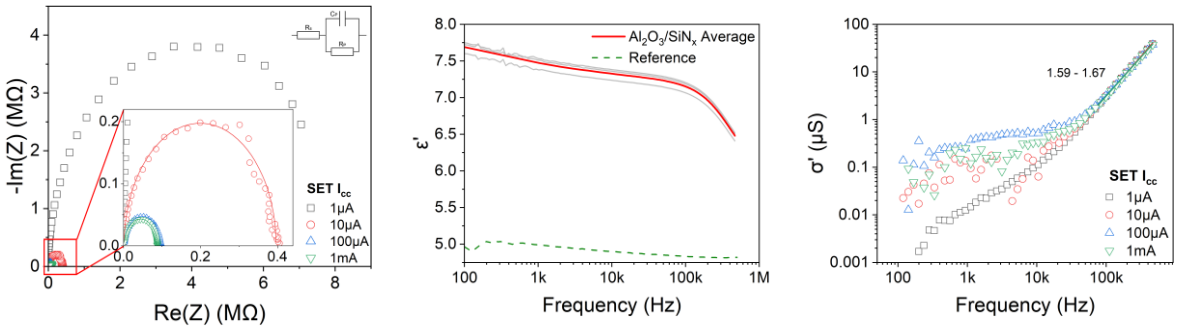

Figure 3 a) Nyquist plots of Al_2O_3/SiN_X devices SET, b) dielectric constant of pristine sample and c) AC conductance of Al_2O_3 sample.