The Dual-Technology FET: nMOS/pTFET in the same device

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Abstract **- This work presents for the first time the experimental results of a Dual-Technology FET (DT-FET). DT-FET is a SOI transistor capable of operating either as an n-type MOSFET (nMOS) or a p-type Tunnel-FET (pTFET), depending on the back gate bias and the source/drain bias conditions. It is an extension of the ^{BE}SOI MOSFET, with the addition of N+ at the drain or source region, which results in different physics of operation depending on back the gate bias. For a positive back gate bias the device behaves as an nMOS, while for a negative back gate bias it behaves as a pTFET. The results were compared with 2D simulations, showing that the overall trends are similar.**

Keywords – Reconfigurable Transistor, nMOS, Tunnel-FET.

I. Introduction

In recent years, the study of reconfigurable transistors has yielded many different structures and technologies [1,2]. Of particular interest to this work is the ^{BE}SOI MOSFET, patented in 2015 [3], which has a very simple fabrication process and depends only on the back gate bias to switch between an n-type or p-type device. Here, we propose a new type of reconfigurability: not only changing the type of the device, but also its main conduction mechanism. Therefore, instead of changing between nMOS or pMOS, we propose a device that switches between nMOS and pTFET. One possible application of this kind of device is to use it as an nMOS for digital circuits and as a pTFET in analog circuits where it is well-known the superior behavior due the lower output conductance presented by silicon-tunnel FETs [4].

II. Device Characteristics

Figure 1 shows the device structure profile and the top view of the fabricated device. Different from the conventional MOSFET structure, one side of the device is left intentionally undoped during the fabrication, so that the back bias may perform the electrostatic doping on it [5]. The fabricated devices have a gate stack of Aluminum, gate oxide of 10 nm, silicon film of 20 nm and buried oxide of 200 nm. On the drain side a phosphorus doping of around 10^{20}cm^{-3} was performed. The channel and the source side are kept with the natural wafer doping of Boron at 10^{15} cm^{-3}. The fabricated devices were also simulated with these same characteristics using a 2D-numerical device simulator (Sentaurus TCAD) in order to see the tendencies observed experimentally in both technology operation. To simulate the tunneling, both Trap-Assisted Tunneling (TAT) and Band to Band Tunneling (BTBT) were considered, using Hurx's model for the TAT and a non-local path for the BTBT.

III. Electrical Characterization and Results

One important remark is that, since the DT-FET is asymmetrical, the definition of drain and source is back gate bias dependent. In Figure 1, two different situations are shown in the schematic representation: if biased as an nMOS (positive back gate bias), a positive drain should be applied to the doped side; if biased as a pTFET (negative back gate bias), a negative drain voltage should be applied to the undoped side.

Figures 2 and 3 present the experimental results of the DT-FET operating as an nMOS, in linear and saturation region respectively, while Figure 4 and 5 show the simulation results, demonstrating that the overall trends are kept, although the numerical values are different, mainly due to the simulated contacts, which were considered to be ohmic, but might not be the case [6]. Besides that, the usual dependency between back gate bias and threshold voltage may be observed in these figures, as should be expected from SOI devices [7], and an average subthreshold slope of approximately 100 mV/dec was extracted.

Figures 6 and 7 show respectively the experimental normalized drain current as a function of the front gate voltage of the DT-FET operating as a pTFET in linear and saturation like region. Figures 8 and 9 present the same results for the simulated devices. Here it must be considered that the series resistance does not have direct impact on the drain current, since the overall current is dominated by the tunneling resistance. Besides that, no ambipolar current is observed both in simulation and experiments, and little variation with respect to the back gate bias is obtained.

The presented results demonstrate that this device, which has a simple fabrication process, is able to operate as nMOSFET or pTFET only changing the applied bias. Considering that this device is manufactured in silicon, with a fully compatible CMOS processing, and knowing the excellent analog potential of Si-TFETs, as a future application it can be proposed that it operates as a MOSFET for digital blocks and as a TFET for analog blocks.

IV. Conclusions

The Dual-Technology FET has been presented for the first time, with experimental results showing that it can operate as an nMOS or as a pTFET depending on the biases applied to the back gate. The experimental observations follow trends similar to those of the simulations, showing that the fabricated devices followed the expected behavior.

Acknowledgment

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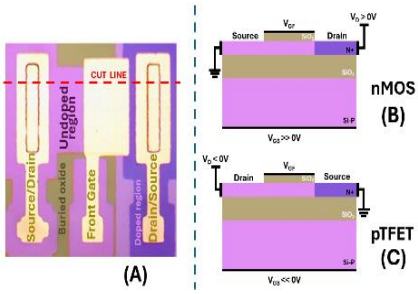

Fig.1– (A) Photo of the fabricated DT-FET (B) DT-FET device structure operating as an nMOS

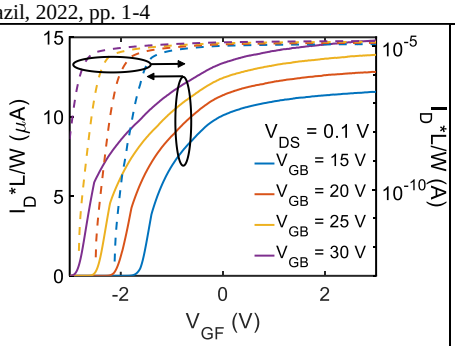

Fig. 2 – Experimental drain current versus front gate voltage for the devices operating as n-type MOSFET with drain biased at 0.1 V.

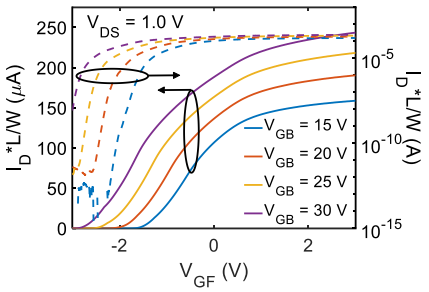

Fig. 3 – Experimental drain current versus front gate voltage for the devices operating as n-type MOSFET with drain biased at 1.0 V

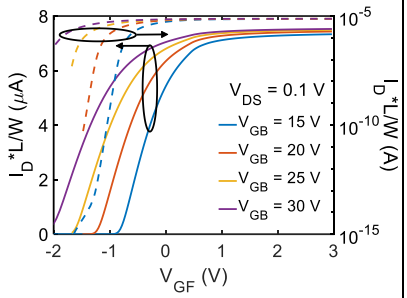

Fig. 4 – Simulated drain current versus front gate voltage for the devices operating as n-type MOSFET with drain biased at 0.1 V

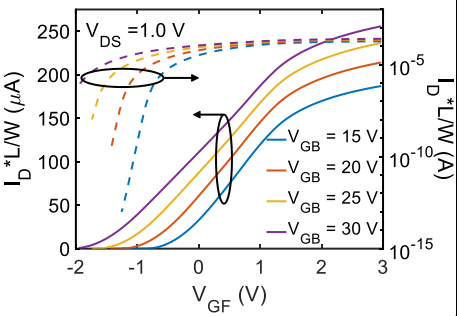

Fig. 5 – Simulated drain current versus front gate voltage for the devices operating as n-type MOSFET with drain biased at 1.0 V

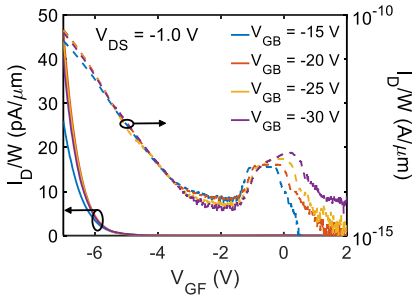

Fig. 6 – Experimental drain current versus front gate voltage for the devices operating as p-type TFET with drain biased at 1 V

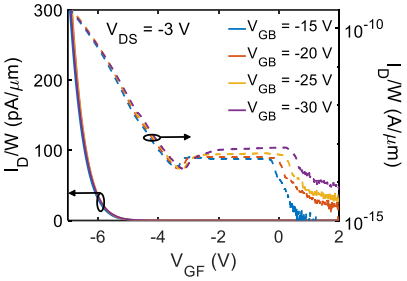

Fig. 7 – Experimental drain current versus front gate voltage for the devices operating as p-type TFET with drain biased at -3 V

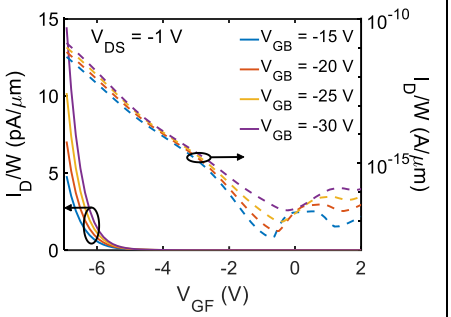

Fig. 8 – Simulated drain current versus front gate voltage for the devices operating as p-type TFET with drain biased at -1 V

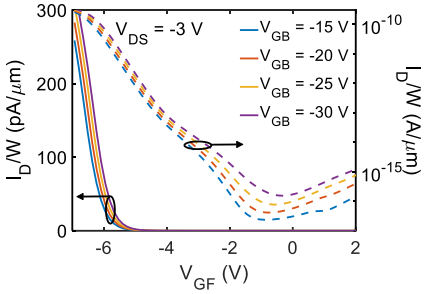

Fig. 9 – Simulated drain current versus front gate voltage for the devices operating as p-type TFET with drain biased at -3 V