Resistive Switching phenomenon in FD-SOI Ω-Gate FETs: transistor performance recovery and back gate bias influence

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Resistive Switching (RS) phenomenon has acquired a lot of interest in the scientific community because its potential use in many applications such as memory, logic, security, neuromorphic systems, etc [1]. Devices where RS is observed are usually named as memristors and, after a forming process, RS provokes a reversible change in the device dielectric conductance between a high and a low resistance state (after a set process) and vice versa (reset process) when a correct bias is applied (Fig. 2B). Usually, memristors are two-terminal capacitive structures, but RS has also been observed previously in FD-SOI quasi-planar transistors [2]. The RS observation in transistors opens the possibility of using the device in a versatile mode as transistor or memristor, as necessary [3]. In this work, for the first time, partial recovery of the transistor characteristics during RS is investigated in N-type FDSOI Ω-gate nanowire FETs with high-k dielectric. On the other hand, other works have observed the influence of the back gate voltage (V_B) in the main parameters of Ω -gate nanowires transistors [4-6], but none of them have analyzed the effect of this biasing on RS, so that, in this work it is also investigated the influence of V_B on RS.

The Ω-gate NW-FETs used in this work were fabricated at CEA-LETI with SOI (Silicon on Insulator) technology, gate length L=10µm and width W=10µm [6]. Their device planar representation and cross-section are shown in Fig. 1A. and Fig. 1B respectively. The great difference between the gate dimensions compared to the nanowire height makes it to be considered as quasi planar SOI MOSFET (Fig. 1C). The electrical measurements were performed with a prober and a Precision Semiconductor Parameter Analyzer Agilent 4156C.

Fig. 2 shows the I_G-V_G measurement after forming (Fig. 2A) and during a complete RS cycle (Fig. 2B). I_D-V_D curves of the fresh sample (Fig. 2C) and after the forming (Fig. 2D), reset (Fig. 2E) and set (Fig. 2F) processes are also represented. Note that transistor functionality is partially recovered after the reset process under the applied electrical conditions (see Fig 2 caption). Fig. 3 shows several RS cycles, obtained with V_B=0V (Fig.3A) and V_B= - 0.2V (Fig.3B). The I_{on}/I_{off} mean ratio calculated at V_G = -1V (see Fig.3A) is 20.08, and 77.9 respectively. This I_{on}/I_{off} ratio increase for larger V_B (in absolute value) improves the distinction between the memristor conduction states, which is beneficial for memory applications.

In summary, this work experimentally studies on the one hand, the I_D-V_D transistor curves during RS stages, which have been partially recovered after the reset process when applying the adequate RS voltages and current limit conditions. This demonstrates the possibility to implement together in a single device a memristor and a transistor. On the other hand, the experimental study of the back gate voltage influence on RS shows that the I_{on}/I_{off} ratio increases with V_B. Future works will explore in more detail these preliminary results.

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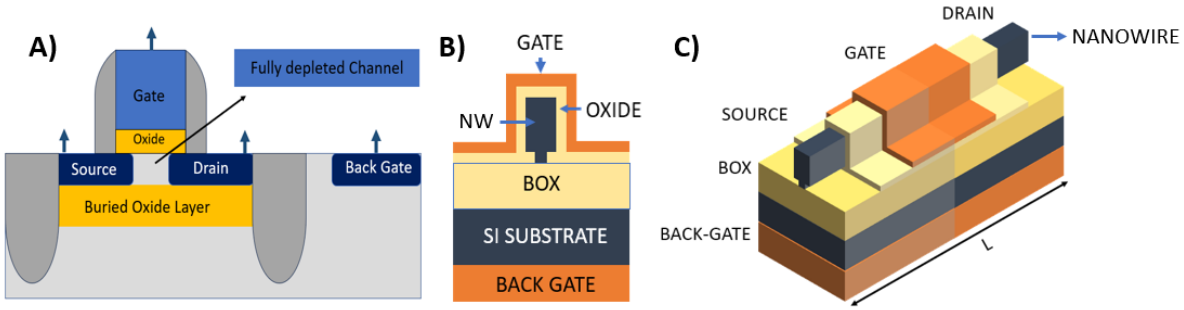

Figure 1. Planar representation of the FD-SOI FET (A) cross section of the Ω-gate Nanowire (B) 3D sketch (non in scale) of the FD-SOI quasi-planar transistors used in this work (C).

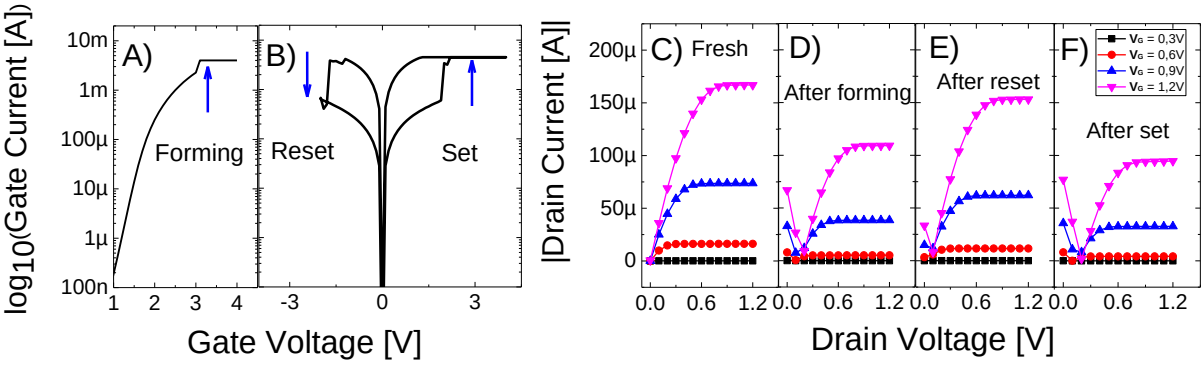

Figure 2. Experimental I_G-V_G curves for A) 'forming' (V_G = 0 to 4V and current limit= 4mA), B) 'reset' (V_G = 0 to -2V and current limit= 8mA) and 'set' (V_G = 0 to 4V and current limit= 4.5mA) processes. I_D-V_D transistor characteristics (V_D = 0 to 1.2V) when (V_G = 0.3V, 0.6V, 0.9V to 1.2V) C) for fresh device. D) after forming. E) after reset and F) after set processes.

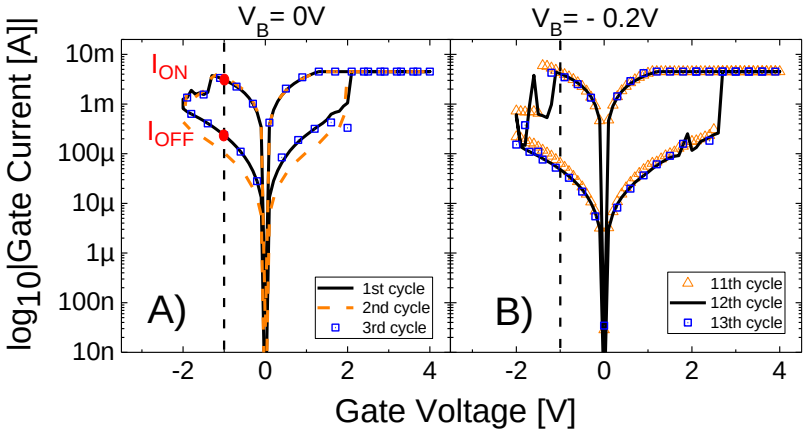

Figure 3. I_{ON}-I_{OFF} ratio measured when A) V_B= 0V, B) V_B= -0.2V.