Non-Uniform matching performances in mesa-isolated SOI MOSFETs

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Abstract— **This work studies the threshold voltage mismatch of mesa-isolated SOI pMOSFETs through a breakdown between edge and center contributions. Pelgrom's law is followed if a proper care is taken in the Vt extraction method. Applied to pMOS devices we observed that despite its parasitic nature, the edge transistor mismatch is as good as that of the center, regardless of channel doping. Even more, the edge mismatch appears to be less degraded when a positive bias is applied to the back-gate.**

I. Introduction

Mismatch in MOSFET transistors plays a crucial role in circuit design [1]. With the scaling down of analog technologies driven by low power application, mismatch origin and modelling have been widely discussed. However, in some specific cases, such as junctionless transistors [2] or mesa-isolated devices, the presence of a parasitic transistor makes a straightforward Vt matching study incomplete. In this context, we discuss a methodology to properly assess the device mismatch and compare main and parasitic transistor performances in our SOI mesa-isolated pMOSFETs.

II. Device description & methodology

SOI pMOS are defined for 2.5V applications such as sensing with channel thickness $t_{si} = 23nm$, burried oxide thickness $t_{box} = 25nm$ and SiO2-Polysilicon gate stack with EOT=6nm. Channel is undoped or doped (8e17at/cm^3, 1.5e18 at/cm^3) to allow multi Vt offer. Due to the mesa isolation, the gate stack covers the complete silicon film, including the edge as shown by TEM cross section on Fig. 1. It was shown in [3] that there are two distinct conduction regimes, one at the edges and one at the center. Thus, the entire device can be modeled as two transistors in parallel. Measurements consisted of I_d-V_g curves in linear regime (V_d=50mV) for three ground plane biases (V_b=-2.5V, 0V, 5V). We measure the V_t standard deviation of pairs of matched transistors $\sigma_{\Delta V_t}$(layout view on Fig. 1.B). Overall devices widths (W_{drawn}) and lengths (L) range from 0.2µm to 25µm.

III. Results and discussion

The edge transistor resulting from the mesa-isolation creates a hump in the I_d-V_g curve (Fig. 2.a), highlighted in the g_m/I_d curve where the highest peak comes from the edge transistor. The edge transistor is always present but not necessarily visible, as demonstrated by the single peak on gm/Id in the undoped channel case (Fig2.b). This stems from the different scaling of each transistor V_t with channel doping and back-gate bias (Fig. 2.b and 2.c). Having identified this issue, it is clear that proper care must be taken in the V_t extraction before getting to mismatch. The most straightforward methods such as extrapolation in the linear region or constant current at $10^{-7}W/L$ do not discriminate between the different regimes. V_t can be that of the edge transistor, of the center, or a mix of both depending on the geometry. The ratio method however [4], applied separately to each peak in the g_m/I_d curves (Fig 2) would be a suitable solution. Instead of the ratio method, in order to cover mismatch in the complete subthreshold regime, we chose to extract V_t at a constant current threshold for several points per decade. At low extraction current, V_t is that of the edge transistor and conversely, extracting at higher currents provides the center transistor V_t. For each threshold current value, we get the corresponding $\sigma_{\Delta V_t}$, leading to Fig. 3. Two plateaus are visible, corresponding to edge and center transistors. At low extraction currents, the two devices W_{drawn} =1µm and W_{drawn} = 25µm have similar $\sigma_{\Delta V_t}$ as expected of the edge transistor, whose dimensions do not scale with the drawn width. At higher currents, there is a x5 difference in $\sigma_{\Delta V_t}$, corresponding to a $1/\sqrt{WL}$ scaling (Pelgrom's law) as expected from a planar SOI transistor. We can get their respective iAvt considering the appropriate $\sqrt{WL}$ ratio. In [3], TCAD simulations showed that the edge conduction regime extends to about 50nm on each side. Therefore, the edge transistor width is the sum of the silicon channel thickness and the 50nm extension on both sides: $W_{edge} = 2(t_{si} + 50) = 150nm$ (Fig. 1). Complementarily, the center transistor width is W_{center}=W_{drawn}-(W_{edge}+2t_{si}). With the appropriate width and $\sigma_{\Delta V_t}$ (Fig. 3), the resulting Pelgrom plot in figure 4 shows a linear variation of $\sigma_{\Delta V_t}$ for both contributions. The straightforward plot with no separate normalization and extraction $10^{-7}W/L$ is also shown for comparison (green squares). The slopes are almost identical for the two devices: same matching performance is achieved (Avt =6mV.µm) for edge and center transistors. We further expand this approach to study the impact of channel doping on center and edge transistor mismatch. Same Avt increase is observed with channel doping for both top and edge transistors, (Fig 5). Finally, we address the back-bias effect on the mismatch for different doping channel. Figure 6 displays $\sigma_{\Delta V_t}$ for three different back-biases (V_b=-2.5V, 0V, 5V). At V_b=-2.5V, $\sigma_{\Delta V_t}$ is constant on the entire current threshold range, indicating that a single transistor is measured instead of two at 0V. Thus, the apparent decrease at low extraction currents is due to a change in conduction regime. On the other hand, at V_b=+5V the two different regimes are maintained and the mismatch of both transistors increases. The increase is much higher in the case of the center transistor, hence the "reverse staircase" shape compared to V_b=0V. This increase in variability for positive back-biases holds true for other dimensions, resulting in the Pelgrom plot figure 7.

IV. Conclusion

We measured matching structures of different dimensions to assess the V_t-matching of pMOS on SOI devices. Because of mesa isolation, a parasitic edge transistor is present. The edge transistor V_t-matching is identical to that of the top transistor with an Avt of 6mV.µm. The impact of channel doping and back bias were investigated. The back bias produced dramatic increase in the V_t-matching with a larger response for the center transistor.

References

[1] P. R. Kinget, "Device mismatch and tradeoffs in the design of analog circuits," in IEEE Journal of Solid-State Circuits, vol. 40, no. 6, pp. 1212-1224, June 2005

[2] D. Bosch, J. P. Colinge, G. Ghibaudo, X. Garros, S. Barraud, J. Lacord, B. Sklenard, L. Brunet, P. Batude, C. Fenouillet-Béranger, J. Cluzel, R. Kies, J. M. Hartmann, C. Vizioz, G. Audoit, F. Balestra, F. Andrieu. "All-operation-regime characterization and modeling of drain current variability in junctionless and inversion-mode FDSOI transistors". 2020 IEEE Symposium on VLSI Technology, Honolulu, HI, USA, 2020, pp. 1-2

[3] A. Boutayeb, C. Theodorou, D. Golanski, P. Batude, L. Brunet, D. Bosch, F. Guyader, S. Joblot, F. Ponthenier, J. Lacord, "Extracting edge conduction around threshold in mesa-isolated SOI MOSFETs," Solid-State Electronics, vol. 209, 2023

[4] A. Ortiz-Conde, F.J. García Sánchez, J.J. Liou, A. Cerdeira, M. Estrada, Y. Yue, "A review of recent MOSFET threshold voltage extraction methods", Microelectronics Reliability, Volume 42, Issues 4–5, 2002

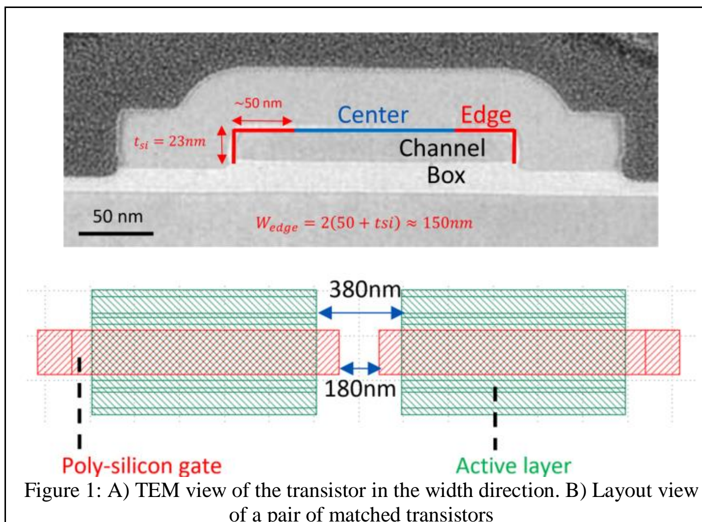

Figure 1: A) TEM view of the transistor in the width direction. B) Layout view of a pair of matched transistors

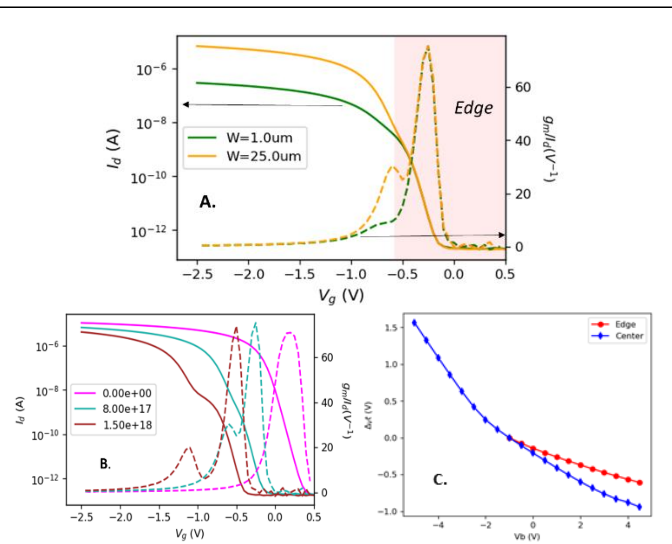

Figure 2: A) Impact of the edge transistor or I_d-V_g and g_m/I_d curves. B) g_m/I_d for different channel doping. C) Dependence of V_t to backgate-bias for both transistors (8e17 atoms/cm^3)

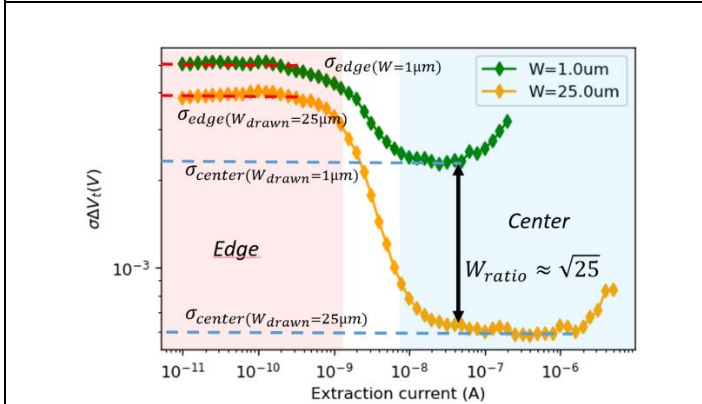

Figure 3: $\sigma_{\Delta V_t}$ as a function of the current threshold chosen for Vt extraction. Doped channel (8e17at.cm²), V_b=0V, L=10µm

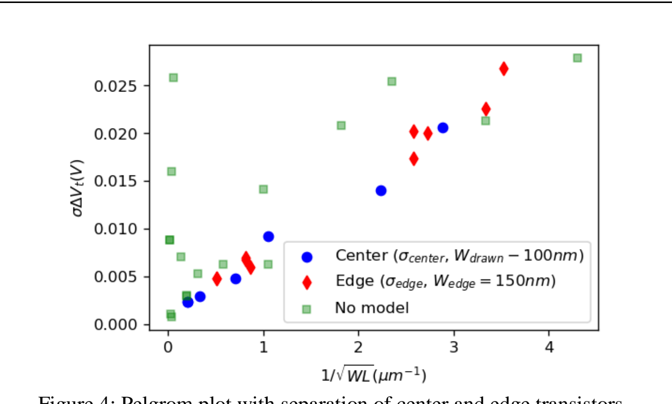

Figure 4: Pelgrom plot with separation of center and edge transistors. Normalized by 150nm for the edge and $W_{drawn} - 100nm$ for the center. (8e17 atoms/cm^3), V_b=0V

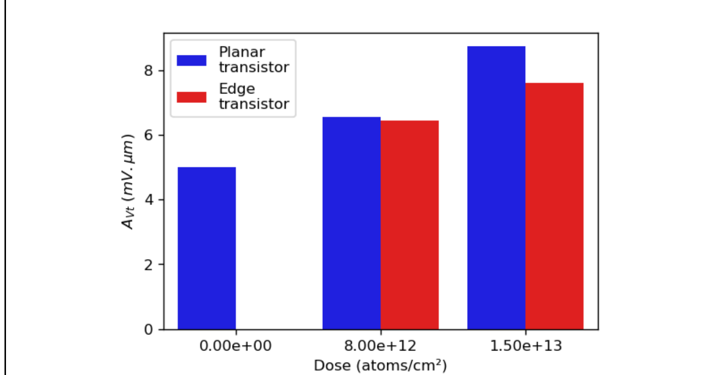

Figure 5: Avt for edge and top transistors at different doping level

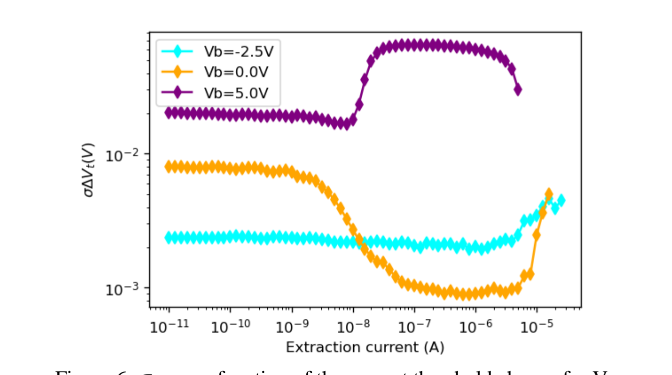

Figure 6: $\sigma_{\Delta V_t}$ as a function of the current threshold chosen for V_t extraction. W=25µm, L=10, Doped channel (8e17 at/cm^3)

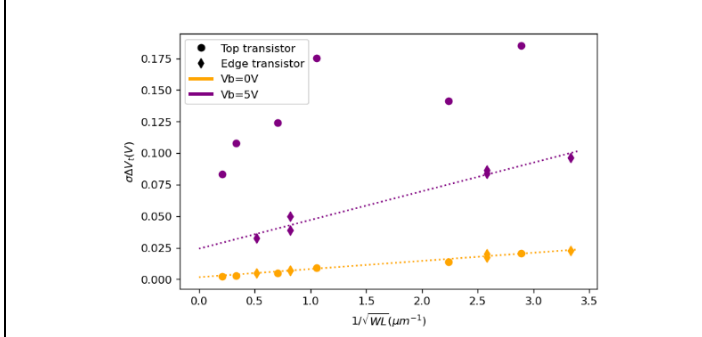

Figure 7: Pelgrom plot with separation of center and edge transistors for V_b=0Vand V_b=5V. 8e17 atoms/cm^3 devices