High-Endurance Bulk CMOS One-Transistor Cryo-Memory

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Most proposed solid-state quantum sensing and computation schemes require cryogenic operation; any large-scale quantum circuitry will need integration with local CMOS-based control, storage, and data processing. We have previously reported on a compact bulk CMOS one-transistor (1T) memory that operates below 10 K via body charging due to impact ionization (II), with long retention times and very high ~10^7 I_1/I_0 memory window in quasistatic measurements [1]. Here we present the endurance and retention characteristics measured at 7 K in high-speed measurements.

Figure 1 summarizes the operating principle of the memory implemented in NMOS: at V_D > 1.5 V, as V_G is swept above V_T, II at the drain creates holes that charge the body to V_B and cannot leave without a low-impedance path to ground. These charges cause a threshold shift, creating positive feedback that switches I_D to a high value. Sweeping V_G back to zero traces out a loop, see Fig. 1(b), with a high ~10^7 ratio between I_1 and I_0 at V_G = 0.3 V. The retention time τ, extracted from the decay of V_B in Fig. 1(c), exceeds 10 minutes at 3 K in quasistatic measurements.

To test the endurance, speed, and retention time, the device was characterized at T ~ 7 K with fast time-domain measurements [2] in a low-T probe station with 50 Ω terminated probes and ~10 ns rise-time voltage pulses, as shown in Fig. 2, together with the write/sense pulse sequence. The fast measurement noise floor was ~0.15 μA, reducing the memory window compared to Fig. 1(b). Even so, a 100 cycle test program yielded a memory window of >1000 X above the noise floor, as shown in Fig. 3(a). Figure 3(b) shows long-term endurance: continuous write '1'/write '0' cycles were applied for 10^3–10^9 cycles, interspersed with the same 100-cycle memory test program. Setting the memory window at 250 X the noise floor, we find the device does not appreciably degrade over 10^9 cycles.

Figure 4 shows the retention time extracted from I_1 current sensing measurements as a function of hold time after write '1' (the '0' state has an uncharged body and is inherently stable, so I_0 is due to the noise floor). If the required I_1/I_0 window is set at 250 X, the retention time τ > 1 s, whereas at 30 X τ > 10 s. These retention times are long on the quantum sensing or computation time scale (a comparable FD-SOI 1T memory using GIDL body charging [3] used a memory window of 2 X). However, they are shorter than τ ~ 800 s obtained in the quasistatic measurement of Fig. 1(c) that used a >10^{14} Ω input impedance electrometer to measure V_B. This difference is due to substrate leakage during measurements as confirmed in Fig. 5, where τ extracted with an added 10 or 100 GΩ input resistor is ~10 s and 56 s. In a 1T memory with no substrate contact we thus expect τ ~ 800 s, essentially nonvolatile.

[1] A. Zaslavsky, C. A. Richter, P. R. Shrestha, B. D. Hoskins, S. T. Le, A. Madhavan, and J. J. McClelland, *Appl. Phys. Lett.* 119 (2021) 043501.

[2] P. R. Shrestha, A. Zaslavsky, V. O. Jimenez, J. P. Campbell, and C. A. Richter, submitted to *J. Electron Dev. Soc.* (2024).

[3] W. Chakraborty, R. Saligram, A. Gupta *et al*., "Pseudo-static 1T capacitorless DRAM using 22nm FDSOI for cryogenic cache memory," in *Intern. Electron Dev. Meeting (IEDM)* (2021) pp. 40.1.1-40.1.4.

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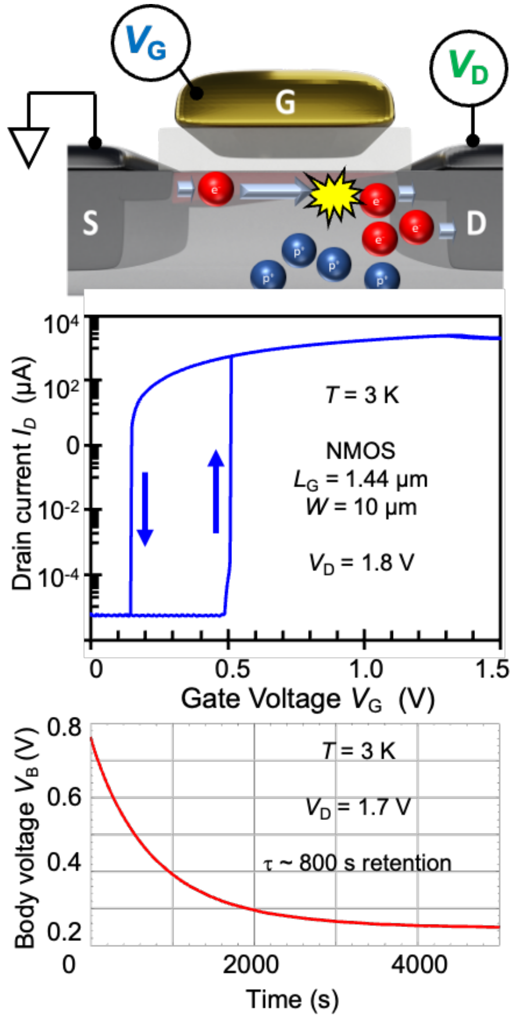

FIG. 1. (a) Schematic diagram of impact-ionization-induced charging of NMOS transistor body with holes for $V_D > 1.5$ V; (b) corresponding hysteretic loop in the $I_D(V_G)$ at $T = 3$ K and $V_D = 1.8$ V; (c) ~10 minute long decay of body potential V_B measured with a >10^{14} Ω input impedance electrometer (adapted from [1]).

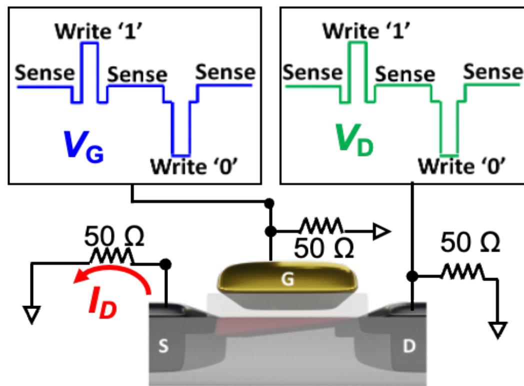

FIG. 2. Schematic high-speed measurement set-up in a cryostat at $T \sim 7$ K together with write '1' ($V_D = 2.1$, $V_G = 1$ V) // sense ($V_D = 1$, $V_G = 0.3$ V) // write 0' ($V_D = 1.5$, $V_G = -1$ V) // sense pulse sequence.

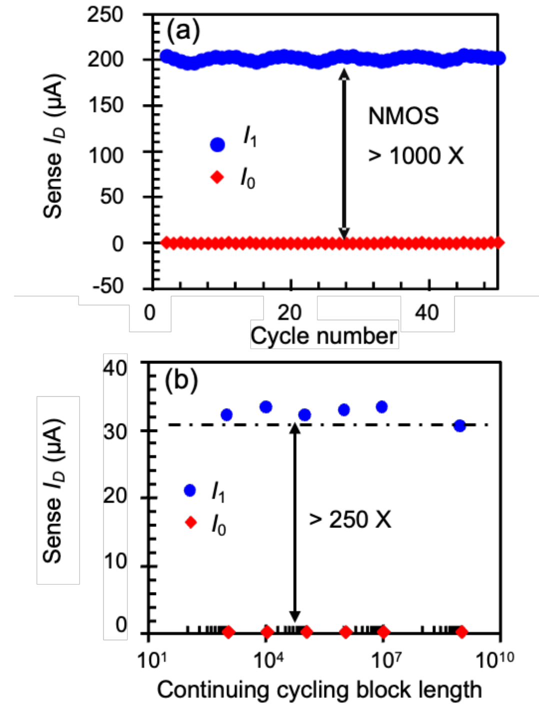

FIG. 3. (a) Raw cycling data for 1T NMOS cryo-memory at ~7 K ($L_G = 0.18$ μm, $W = 10$ μm), with I_1 sense current exceeding the ~0.15 μA I_0 noise floor by >1000 X; (b) long term endurance cycling with continuous multiple write '1'/write '0' cycle blocks ranging from 10^3 to 10^9 in order of magnitude steps followed by 100-cycle memory test program as in (a).

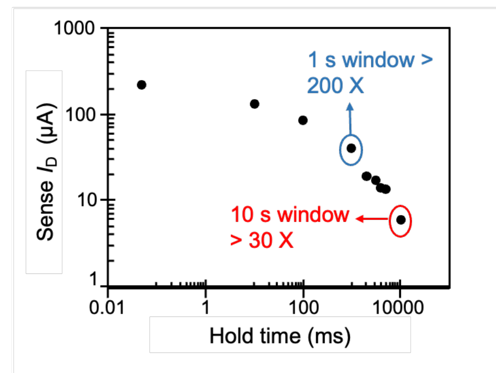

FIG. 4. Lower bound on retention time τ extracted from I_1 sense measurements after hold times of 100 μs to 10 s in order of magnitude steps.

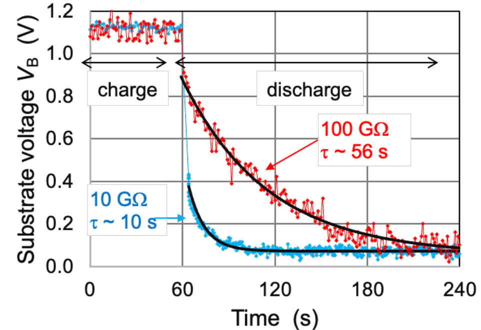

FIG. 5. Measured retention τ dependence on the input impedance of the measurement system.