Enhancing Cryogenic Performance of FDSOI Logic Circuits Using Back Biasing and Threshold Voltage Engineering

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Introduction: The demand for low temperature circuits in various applications, including space electronics, data center power reduction, and quantum computing, necessitates the re-design and verification of the Room Temperature (RT) circuits designed for operation at cryogenic temperatures. Threshold voltage (Vth) increase with the temperature reduction is a major challenge, which can significantly affect circuit operation. This paper investigates the impact of back biasing and threshold voltage engineering on the performance of FDSOI based circuits at cryogenic temperatures. Additionally, we explore supply voltage (V_{DD}) reduction for power budgets and propose Vth engineering as a solution to optimize power/speed trade-offs.

Methodology: Predictive cryogenic spice compact models are developed for 22nm FDX technology using re-centering [1] of RT Process Design Kit (PDK) based on experimental measurement data and TCAD simulations across process corners and statistical variations to simulate the most likely behavior of circuit performance at low temperatures [2]. The re-centering procedure is necessary as the PDKs from the foundries are tailored for room temperature usage, and there are currently no available foundry PDKs designed specifically for cryogenic temperature applications. For the benchmarking of the circuit performance, we used a conventional 7-stage Ring Oscillator (RO).

Results and Discussion: The ring-oscillator circuit simulations are used to extract propagation delay and power dissipation per stage. The results obtained without using any back bias are summarized in Table 1. We observe reduced power per stage but increased propagation delay and reduced frequency at 4K compared to room temperature (300K). ***Impact of V_{DD} Reduction:*** Next, we reduce the supply voltage, and its impact on reducing the frequency and power dissipation is shown in Fig. 1 for the RO based on the TT corner devices for 300K and 4K cases with no back gate bias. Fig. 2 illustrates the higher Vth at 4K compared to 300K. The reduction in Vth when applying back bias is also demonstrated for 4K with the magnitude of back bias, $|V_{BG}|$ varying from 0 to 2V. ***Impact of Back Bias:*** We explore the impact of the back bias on the circuit performance, and the delay and power per stage as a function of V_{DD} and the results are shown in Fig. 3. ***Impact of Vth Engineering:*** We first reduce the Vth at 4K at zero back bias so as to match the off-state leakage at RT, and the results are shown in Fig. 4 including subsequent simulated characteristics at 4K with varying V_{BG}. RO simulation results are shown in Fig. 5, and we note that: (a) V_{DD} must be reduced at 4K to avoid increase in power dissipation, (b) maximum V_{BG} is always best for speed but may not be best when trading off speed vs power, and (c) the "sweet spot" is around V_{DD}=0.4V, V_{BG}=1V.

Conclusions: To achieve significant power reduction at cryogenic temperatures, a combination of back biasing and threshold voltage engineering is crucial. Back bias alone offers a maximum of 60% power reduction compared to RT, while the combined approach yields up to 4.5 times power reduction.

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References: [1] L. Wang et al., "TCAD proven compact modelling re-centering technology for early 0.x PDKs," *SISPAD 2016*, pp. 157-160, 2016. [2] T. Dutta et al., "A Methodology for PDK Re-Centering Using TCAD and Experimental Data for Cryogenic Temperatures", unpublished. [3] Sentaurus Device Manual, *Synopsys Inc.*, Mountain view, CA, USA, 2022. [4] HSPICE User Guide, *Synopsys, Inc.*, Mountain view, CA, USA, 2022.

Table1: RO simulation at RT and 4K.

	T=300K	T=4K
Delay/stage (pS)	2.74	2.93
Power/stage (µW)	11.40	10.47
Frequency (GHz)	26.18	24.30

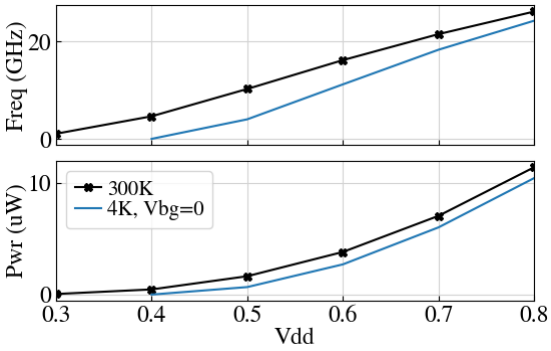

Fig. 1. Frequency and power per stage for V_{BG}=0V at TT corner.

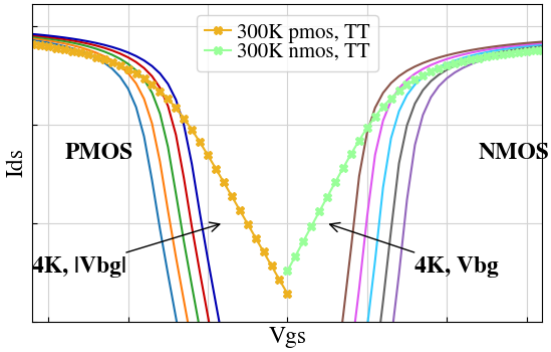

Fig. 2. I_D-V_G characteristics with back-gate voltage (V_{BG}) sweeps at 4K, and 300K results for reference (TT case).

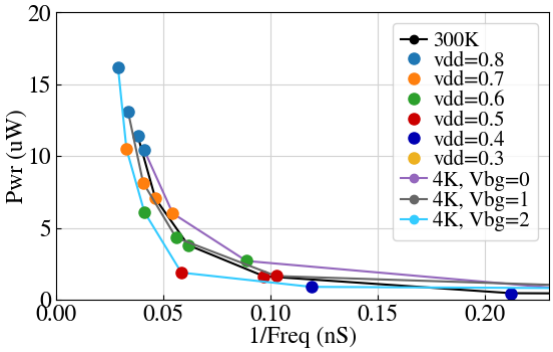

Fig. 3. Delay Vs Power dissipation for different V_{DD} and $|V_{BG}|$.

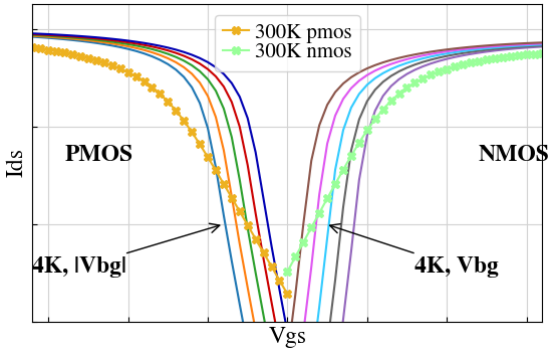

Fig. 4. Adjusted I_D-V_G at 4K to match Ioff at 300K, and subsequent impact of $|V_{BG}|$.

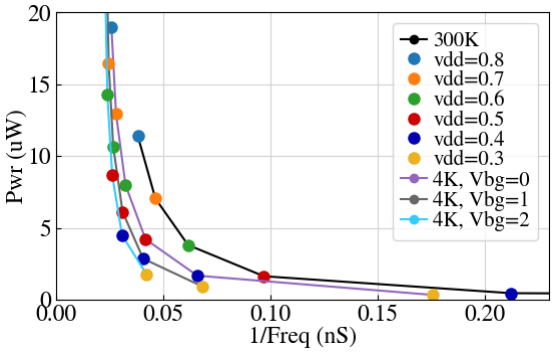

Fig. 5. Delay Vs Power dissipation for different V_{DD} using the Vth engineered devices under different $|V_{BG}|$.