Back Bias Effect with Hysteresis in Cryogenic 200 nm SOI MOSFETs

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Introduction Quantum computers, such as superconducting and spin-based, control qubits at millikelvin temperatures from room-temperature control systems, but problems such as the physical limits of wiring and heat influx arise when making more multi-qubits. Therefore, placing CMOS integrated circuits (cryo-CMOS) in cryogenic environments has recently attracted attention. The cryo-CMOS must also operate with low power consumption due to meet the refrigerator's cooling budget. SOI MOSFET technology is the promising candidate to reduce the power consumption because it has a back gate that can reduce the threshold voltage (V_t), even with V_t increasing at low temperatures. Previous work also shows the possibility of the low power with SOI MOSFET [1]. This study focuses on the back gate effect of SOI MOSFET and reports new finding of hysteresis effects.

Device Structure and Measurement Results Fig. 1 shows the device structure and parameters of the N-channel SOI MOSFET. The devices were fabricated using LAPIS Semiconductor 200 nm SOI CMOS process. We prepared two types of devices, RV_t (Regular V_t) and LV_t (Low V_t), in which the V_t's were controlled by varying the impurity concentration.

Fig. 2 shows the temperature and V_{sub} dependence of the LV_t device. V_t increases with decreasing temperature, and the increased V_t is then compensated by V_{sub}. Fig. 3 and 4 show the results of continuous measurements (two cycles) of V_{sub} = 0–10 V at 3 K. In the second measurement (2nd), the characteristics of the subthreshold region at V_{sub} = 0–4 V differ from those of the first measurement (1st). Fig. 5 shows the maximum V_{sub} and ambient temperature dependence. The hysteresis gradually disappears when the maximum V_{sub} is decreased and the temperature is increased. Fig. 6 shows the verification of the conditions under which the device returns to its 1st state. The hysteresis does not occur when there is a long interval between the 1st and 2nd measurement or the temperature was raised to 300 K, and then the 2nd measurement was carried out.

Discussion We consider that the above results are caused by the traps of the Box side, which only works at cryogenic temperatures. When the Box side is strongly inverted (V_{sub} < 8 V) at cryogenic temperature (< 10 K), carriers flowing to the back gate side could generate traps, and also carriers are trapped (Fig. 7(a)) and these induce the hysteresis effect (Figs. 3–5). However, the trapped carriers are detrapped depending on the return action to room temperature and the interval time (Fig. 6). The shoulder shape characteristics suggest the presence of low V_t locations within the device, which could be caused by the hole trap as shown in Fig. 7(b).

Conclusion We found out that the back bias in the cryogenic SOI MOSFET induced the hysteresis effect. This phenomenon must be considered in circuit design and parametric tests.

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References [1] H. Bohuslavskyi *et al.*, *IEEE T-ED*, vol. 65, no. 9, pp. 3682-3688, Sept. 2018.

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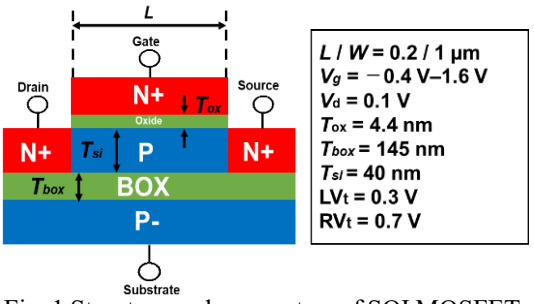

Fig. 1 Structure and parameters of SOI MOSFET.

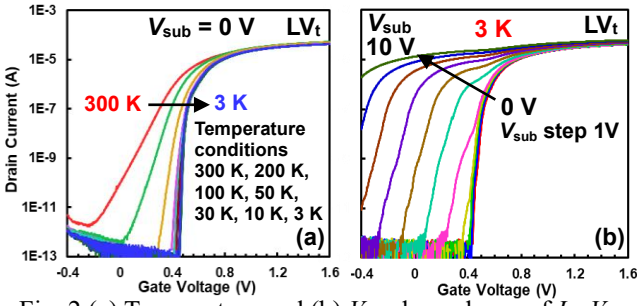

Fig. 2 (a) Temperature and (b) V_{sub} dependence of I_d–V_g.

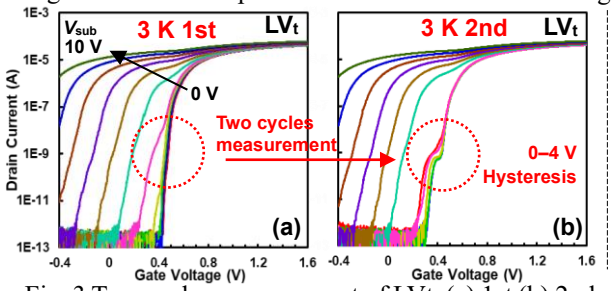

Fig. 3 Two cycles measurement of LVt. (a) 1st (b) 2nd.

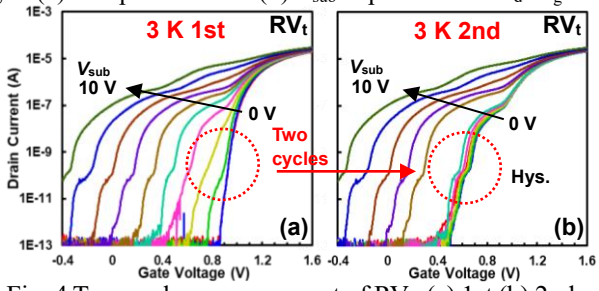

Fig. 4 Two cycles measurement of RV_t. (a) 1st (b) 2nd.

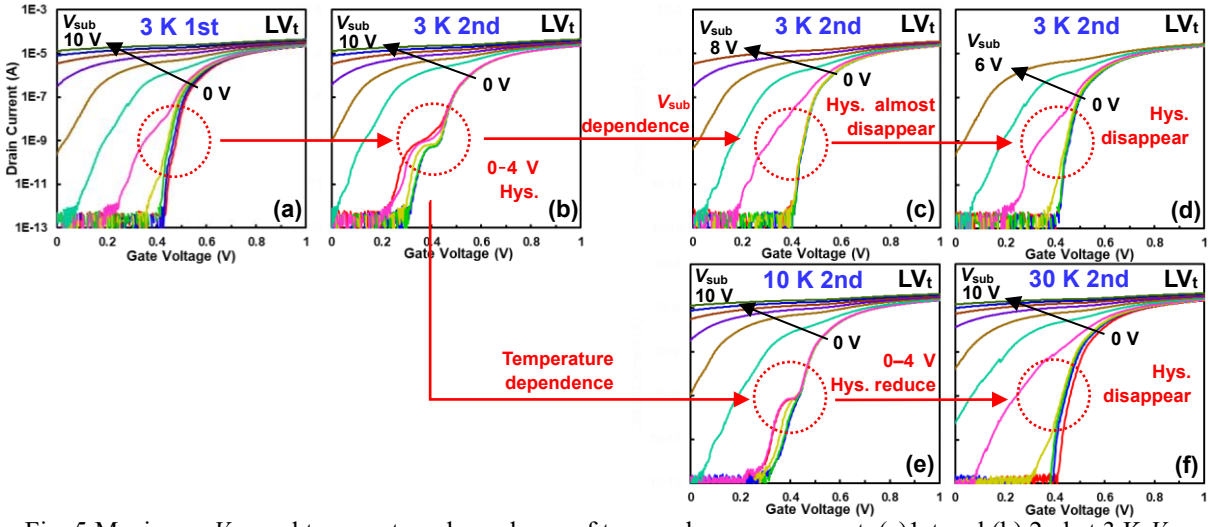

Fig. 5 Maximum V_{sub} and temperature dependence of two cycles measurement. (a)1st and (b) 2nd at 3 K V_{sub} = 0–10 V. (c) V_{sub} = 0–8 V 2nd and (d) V_{sub} = 0–6 V 2nd. (e) 10 K 2nd and (f) 30 K 2nd.

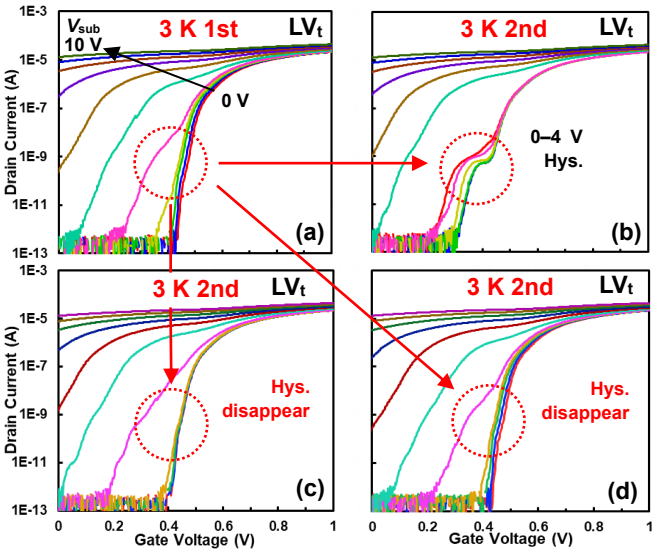

Fig. 6 Two cycles measurement (a) 1st, (b) 2nd, (c)with interval time (approximately 6 hours), and (d) via room temperature (300 K).

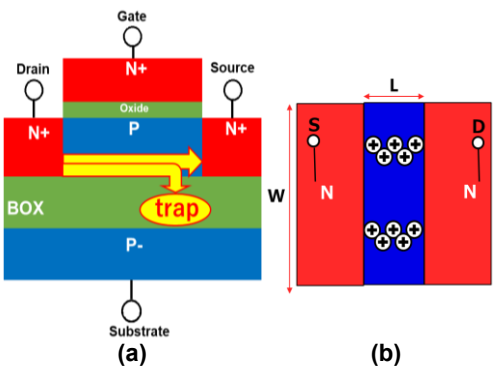

Fig. 7 Illustration of expected mechanism. Trap is generated when substrate bias is applied (a). Trap location dependence (b).