Analog Behavior of Forksheet at High Temperatures

Joao A. Martino[1*], Paula G. D. Agopian[1,2], Julius Andretti[1], Romain Ritzenthaler[3],
Hans Mertens[3], Anabela Veloso[3], Naoto Horiguchi[3]
[1] *LSI/PSI/USP, University of Sao Paulo, Sao Paulo, Brazil*
[2] *UNESP, Sao Paulo State University, Sao Joao da Boa Vista, Brazil*
[3] *imec, Leuven, Belgium*
email*: martino@usp.br

Abstract - **This work presents the analog behavior of n-type forksheets from room to 150ºC with channel lengths of 26 and 70 nm. These devices present a Zero Temperature-Coefficient (ZTC) point for gate voltage around 0,59 V (V_{ZTC}) in saturation region. The threshold voltage variation with temperature (dV_T/dT) is around -0,5mV/ºC due to the Fermi level decrease. The DIBL increase with temperature but it is kept lower than 51mV/V in the studied temperature range. The transconductance and output conductance decrease (mainly due the mobility degradation) which results in an intrinsic voltage gain around 36 dB, showing a slight change (±2dB) in the studied temperature range. The maximum unit gain frequency was estimated around 3.87 GHz in strong inversion regime. The results show that the forksheet can also be used for analog applications at high temperature, in addition to the already known savings in footprint area compared to nanosheet technology.**

Keywords – Forksheet, Analog Parameters, High Temperature.

I. Introduction

The continuous downsizing of CMOS technology and the need to improve device performance have motivated the evolution of transistor structures from FinFETs to nanosheets [1-3]. However, with the search for a smaller footprint area in the integrated circuit, devices that integrate n and p-type transistors in the same structure have attracted the attention of the scientific community. Keeping it in mind, the complementary FETs (CFETs) [4] and forksheet [5] structures have been studied. CFET are obtained by stacking n and p-type nanosheets on top of each other, while in the forksheets the n and p-type transistor are separated by a lateral dielectric wall [6].

Complementary to the study presented in [7, 8] where the basic forksheet parameters were studied, this work focuses on analyzing the potential of forksheets for analog applications at high temperatures.

II. Device Characteristics

The forksheets were fabricated in imec/Belgiun with the details shown in [7**,** 8]. The forksheet schematic structure and TEM image can be seen in Fig.1. The devices used in this work are n-types with silicon thickness of H_{FS} = 7nm, silicon width of W_{FS} = 23 nm, $W_{eff} \cong$ 212 nm $(2.W_{FS} + H_{FS})$x4, layout gate length of L_G = 26 and 70 nm. These devices were submitted at 25ºC, 100ºC and 150ºC. The gate stack is based on HfO_2 (high-k) and TiAl (eWF layers) with EOT ≅ 1.1 nm. Only for an estimation of the unit gain frequency (f_T), it was used a p-type forksheet with large dimensions with L_G = 250 nm and W_{eff} = 31200 nm.

III. Electrical Characterization and Results

The electrical characterization of forksheet was performed using the Semiconductor Parameter Analyzer B1500 [9]. Fig. 2 shows the drain current (I_D) as a function of gate voltage (V_{GS}) in saturation region showed in linear and logarithm scale from room up to 150ºC. It is possible to observed the presence of Zero-Temperature Coefficient point (ZTC) where V_{ZTC} (V_{GS} at ZTC point) is around 0,59 V in saturation region (V_{DS}=700mV). The presence of ZTC is good for analog application. For many analog circuit applications, it is desirable to bias the devices at a point in a circuit where the voltage/current show a very little or no variation with temperature, i.e. in ZTC point. The presence of ZTC is related to the competition between the decrease of threshold voltage (V_T) and the degradation of carrier mobility (μ) when the temperature increase. For $V_{GS} < V_{ZTC}$ the V_T is the dominant factor on I_D value and for $V_{GS} > V_{ZTC}$, the μ is dominant. It is worth noting that not all devices present ZTC point. For example, the Junction-Less Transistors did not present ZTC point due to the very high series resistance, which strongly degrades the I_D and the degradation caused by temperature is not enough to overcome the increase in I_D caused by the V_T decrease, and as a consequence no ZTC is reached.

Fig.3 shows the V_T and DIBL (Drain Induced Barrier Lowering) as a function of temperature for forksheet with L_G of 26 and 70 nm. The dV_T/dT on the n-type forksheet is around -0,5mV/ºC, due to the Fermi level decrease, which is also the value observed for these devices observed from room down to 4 K [10]. The DIBL increase with the temperature but it is still low in the studied temperature range (DIBL is 51 mV/V in the worst case).

The subthreshold swing (SS) as a function of temperature (T) is shown in Fig.4. For both analyzed channel lengths, the experimental SS satisfactorily follows the ideal theoretical trends, increasing from ~62 mV at 25ºC to ~97 mV/dec at 150ºC in saturation regime. The maximum transconductance (gm_{MAX}) in linear region and the saturation transconductance (gm_{SAT} at V_{GT} = 200 mV) as a function of temperature for two channel lengths are shown in Fig.5. Both gm decrease with temperature due to the μ degradation as expected. The ratio between the gm(26nm)/gm(70nm) is lower than 2,7 (70/26) due to the fact that the effective channel length is higher than the gate layout related to the gate last process.

The forksheet transistor efficiency (gm/I_D) for different temperatures and two channel lengths is presented in Fig. 6. In weak inversion ($I_D < 10^{-8}$) the gm/I_D is inversely proportional to SS shown in Fig.4, which explain the reason for the decrement of the transistor efficient with the temperature. No relevant difference is observed for both channel lengths.

The output conduction (g_D) and Early voltage (V_{EA}) as a function of temperature for two channel lengths is shown in Fig.7. The extraction of these parameters was done at V_{DS} = 700mV and V_{GT} = 200 mV from I_D x V_{DS} curve, which is very noisy and may introduce some additional errors.

The Intrinsic voltage gain (A_V) as a function of temperature for two channel lengths is obtained ($A_V = 20.\log(gm_{SAT}/g_{D,SAT})$) and presented in Fig.8. For L_G=70nm the A_V is higher than L_G=26 nm due to the higher V_{EA}. The A_V variation with the temperature is not higher than ±2dB in the studied temperature range.

The unit gain frequency (f_T) as a function of drain current was estimated using a large pFET forksheet devices (L_G=250nm and W_{eff}=42800 nm) and $f_T \cong gm_{SAT}/(2.\pi.Cgg)$, where Cgg is the gate capacitance. The maximum f_T value got is 3.87 GHz at I_D=429μA (strong inversion). The f_T value may be slightly overestimated thanks to the lower Cgg value due to the high series resistance in the capacitance extraction.

The results show that in addition to the known savings in footprint area of forksheet compared to nanosheet technology (which is estimated to be around 20% lower area for logic circuit and 30% for SRAM [5]), the forksheet devices can also be used for analog applications from room to 150ºC.

IV. Conclusions

This work presents the analog behavior of forksheets from room to 150ºC. N-type forksheets with channel lengths of 26

and 70 nm were analyzed. These devices present a Zero Temperature-Coefficient point for a gate voltage around 0,59V in saturation region. The threshold voltage variation with temperature (dV_T/dT) is around -0,5mV/ºC which is the typical value for fully depleted multigate devices. Similar results for dV_T/dT were also observed in the literature for forksheet at low temperatures. The DIBL increase with temperature but it is kept low (< 50mV/V) in the studied temperature range. For both analyzed channel lengths, the experimental SS satisfactorily follows the ideal theoretical trends, increasing from ~62 mV at 25ºC to ~97 mV/dec at 150ºC in saturation regime. The transconductance and output conductance decrease due to the mobility degradation with the temperature increase. The intrinsic voltage gain of 36 dB was obtained and a slight change of ±2dB is obtained from 25ºC to 150ºC. The results show that the forksheet can also be used for analog applications in the studied temperature range, in addition to the known savings in footprint area compared to nanosheet technology.

ACKNOWLEDGMENT

The Brazilian authors acknowledge CNPq, CAPES and São Paulo Research Foundation - FAPESP (under grant #2020/04867-2) for the financial support. We also thanks imec CMOS technology program members and the amsimec test labs for their support.

REFERENCES

[1] Dash, T.P. et al., Toward Ultimate Scaling: From FinFETs to Nanosheet Transistors. In: Green Technology for Smart City and Society. Lecture Notes in Networks and Systems, vol 151. Springer, Singapore.2021, https://doi.org/10.1007/978-981-15-8218-9_19

[2] Collaert, N.. From FinFET to Nanosheets and Beyond. In: Handbook of Semiconductor Devices . Springer Handbooks. Springer, Cham. 2023, https://doi.org/10.1007/978-3-030-79827-7_7

[3] N. Loubet et al., "Stacked nanosheet gate-all-around transistor to enable scaling beyond FinFET," 2017 Symposium on VLSI Technology, Kyoto, Japan, 2017, pp. T230-T231, doi: 10.23919/VLSIT.2017.7998183.

[4] S. -G. Jung, D. Jang, S. -J. Min, E. Park and H. -Y. Yu, "Performance Analysis on Complementary FET (CFET) Relative to Standard CMOS With Nanosheet FET," in IEEE Journal of the Electron Devices Society, vol. 10, pp. 78-82, 2022, doi: 10.1109/JEDS.2021.3136605.

[5] P. Weckx *et al.*, "Novel forksheet device architecture as ultimate logic scaling device towards 2nm," IEDM Tech. Dig. 2019.

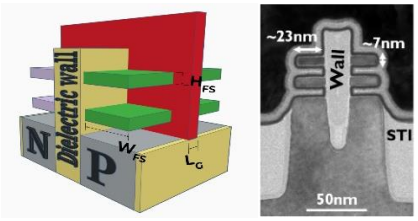
[6] https://semiengineering.com/knowledge_centers/integrated-circuit/transistors/3d/forksheet-fet/

[7] H. Mertens et al., "Forksheet FETs for Advanced CMOS Scaling: Forksheet-Nanosheet Co-Integration and Dual Work Function Metal Gates at 17nm N-P Space," 2021 Symposium on VLSI Technology, 2021.

[8] R. Ritzenthaler et al., Comparison of Electrical Performance of Co-Integrated Forksheets and Nanosheets Transistors for the 2nm Technological Node and Beyond", IEDM 2021.

[9] Keysight Technologies, B1500 *Technical Data Sheet 2023*

[10] R. Asanovski et al., Characterization of DC Performance and Low-Frequency Noise of an Array of nMOS Forksheets from 300 K to 4K, EUROSOI-ULIS 2023.



(a) (b)

Fig.1– Forksheet: (a) Schematic view and (b) TEM image perpendicular to the gate channel [7].

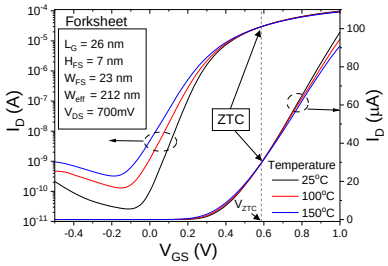


Fig.2 – Drain current as a function of gate voltage for different temperatures

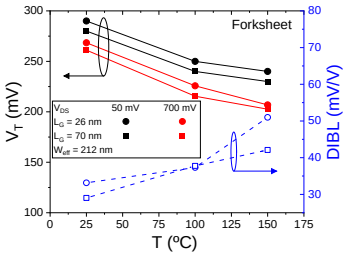


Fig. 3 – Threshold voltage and Drain-Induced-Barrier-Lowering as a function of temperature for two channel lengths.

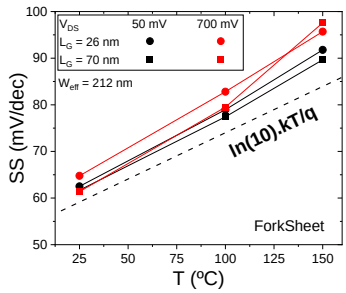


Fig. 4 – Subthreshold swing as a function of temperature for two channel lengths.

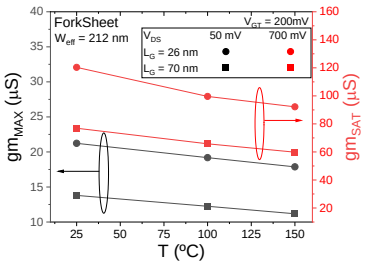


Fig. 5 – Transconductance in linear (maximum point) and saturation region (at V_{DS} = 700mV and V_{GT} =200mV) as a function of temperature for two channel lengths.

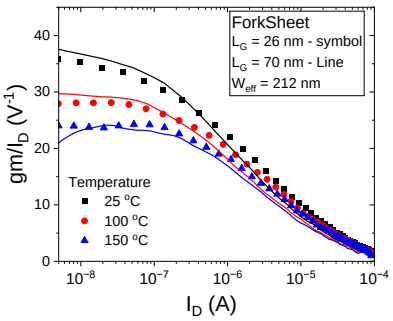


Fig. 6 – Transistor efficiency for different temperature and two channel lengths.

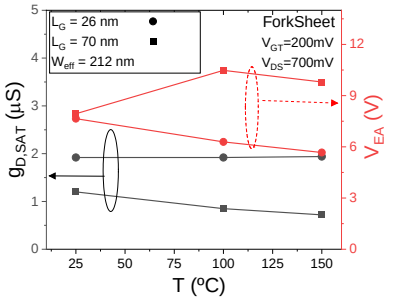


Fig. 7 – Output conduction and Early voltage as a function of temperature for two channel lengths.

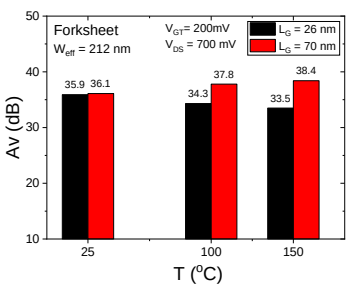


Fig. 8 – Intrinsic voltage gains as a function of temperature for two channel lengths.

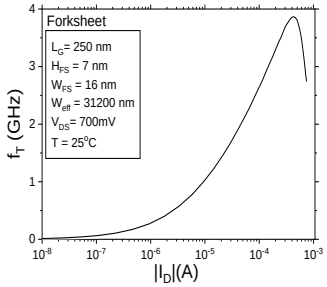


Fig.9 – Unit gain frequency as a function of drain current obtained from a large pFET forksheet dimension