# Preliminary numerical study on magnet gate in MOS FD-SOI for quantum and sensor applications

Philippe Galy<sup>1</sup>, Franck Sabatier<sup>1,2,3,4</sup>, Fabien Ndagijimana <sup>3</sup>, Dominique Drouin<sup>2,4</sup>

[1] STMicroelectronics, 850 rue Jean Monnet, 38920 Crolles, France

[2] Laboratoire Nanotechnologies Nanosystèmes (LN2) CNRS UMI-3463—31T, CNRS, Sherbrooke J1K 0A5, Canada

[3] Grenoble Electrical Engineering Laboratory (G2elab), Grenoble Alpes University (UGA), 38031 Grenoble, France
[4] Institut Interdisciplinaire d'Innovation Technologique (3IT), Université de Sherbrooke, Sherbrooke, Québec J1K 0A5, Canada

#### Abstract:

This preliminary study aims to report a possible new MOS device with a stack of magnetic gates, for example in 28 nm FD-SOI UTBB technology. This study focuses on a proposed stacking in a MOS gate through 3D HFSS numerical simulations to evaluate the magnetic field gradient under and around the MOS device. Typically, the polycrystalline gate is replaced by a magnetic material with metallic behavior to also enable conventional electrostatic MOS control. The dimensions meet 28nm design requirements and Co or Ni magnetic materials are candidates for process integration. In addition, other materials should be selected based on the magnetic specifications and metal work function. Applications could be with an internal or external magnetic field environment for quantum or sensor applications. 3D magnetic simulations are carried out with the HFSS tool.

## Keywords- FD-SOI CMOS, cryogenic temperatures, 3D FEM simulation

## I. INTRODUCTION

The purpose of this article is to report the main numerical results on a combo function at the MOS gate level in FD-SOI technology for quantum or sensor applications. One of the promising candidates is FD-SOI technology which today demonstrates relevant performances in low power consumption for RF/analog/digital design at cryogenic temperature. Therefore, 28nm ultra-thin body buried oxide (UTBB) fully depleted silicon-on-insulator (FD-SOI) technology is explored based on these typical dimensions, materials, and process steps. Figure 1 gives a cross-section view of a MOS device and shows the typical gate stacking process with a 2D MOS TCAD shape. From top to bottom, the stack consists of a silicide (CoSi2) contact on a polycrystalline silicon (p-Si) gate pillar, followed by a metal (TiN) gate compatible with the middle of the silicon band gap which is on a high k dielectric. This high k hafnium (HfO2) is the gate oxide (Tox). Afterwards, we find a thin silicon film (Si film) for the electronic channel which is placed on a buried oxide (Box) and which is on a bulk silicon substrate (Handle substrate). MOS electrostatic control is provided by the metal work function, by the top gate voltage and if necessary, by the additional back gate bias. For a qubit and for example, EDSR control requires a magnetic field gradient close to the qubit that could be integrated into the back end of the line (BEOL) with a Co micromagnet or other magnetic material. A 3D quantum TCAD simulation on an ideal topology result in a Rabi frequency of  $f_R = 4.7$  MHz. However, the micromagnet is quite far from the area of interest and minimizes the impact of the magnetic field gradient. The main idea here is therefore to replace a part of the gate stack (silicide/poly/metal grid) with a magnetic material with metallic behavior and which complies with the work function for the MOS electrostatic control. Figure 2 shows a top view of a possible standalone qubit where the quantum dot is at the center of the device. Also reported is a 2D HFSS (z-axis) view of the device stack with a zoom in on the Co/Tin/HfO2 /Si/Box/Si structure as a first device proposal. Figure 3 gives the two types of devices studied where the metal gate is the TiN or Co material. In this case, a 100 mV offset of the metal work function is between these two metals. This voltage offset could be restored by biasing the back gate and maintaining the control of the initial front gate voltage. Figure 4 gives for structure #1 the vector mapping of the magnetic field and the magnitude mapping centered on the quantum dot in two conditions: for the vertical and horizontal orientation of the magnetic field of the micromagnet with 1T (au). Numerical simulation extractions in both cases show that the gradient is well below the gate MOS in the quantum dot and that the magnetic spreading is consistent with the dimensions of this device. The following figure 5 concerns structure #2 where the metal gate is a ferromagnetic material, here Co. We extract from the previous one that the magnitude is 4% higher than the previous case due to the shield of TiN. Thus, the two process solutions could be integrated without major change in device behavior (except reverse bias if necessary). Furthermore, for (accurate study of the magnetic gradient mapping in the entire device, several Z-cut planes are extracted and presented in Figure 6. In conclusion, a micromagnet embedded in the gate stack with suitable magnetic material and electrical conductivity is a future way to enable efficient electrostatic control of the MOS device as a quantum dot function and provide a magnetic gradient for the spin control via the EDSR technique. Additionally, the material hysteresis curve is an important feature for Hc and Hr values as a function of the external magnetic magnitude of the Zeeman effect required for spin manipulation.

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Figure 1: a) FD-SOI MOS cross section, b) TCAD MOS transistors with gate stack .



Figure 2: a) top view on a standalone Qubit Layout in 28FD-SOI b) 2D view in HFSS in z axe c) zoom in stack : Co/TiN/HfO2/Si/Box/Si



Figure 3: a) Stack structure #1 : Co/TiN metal gate b) stack structure #2 Co/Co metal gate (all other elements are kept identically)



Figure 4: a) Vertical mapping of magnetic vector and magnitude b) Horizontal mapping of magnetic vector and magnitude (1T au)



Figure 5: a) Stack structure #2 with Zoom in and with vector /magneitude map extractions



Figure 6: cut plan extractions for differente deepth z=0 ; 2,5 ; 32,28 & 38,5 nm

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