TLM-based numerical extraction for CMOS-compatible N^+-InGaAs ohmic contacts on 200mm Si substrates

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Abstract – We report the results of a TLM-based numerical extraction methodology applied on CMOS-compatible n^+-InGaAs ohmic contacts integrated with dielectrics on 200mm Si substrate. We obtained state-of-the-art level ρ_c = 7,5.10^{-8} ohm.cm² for relevant contact dimensions (THz HBT for 6G). This methodology is first described and calibrated using contacts on SOI.

Introduction

As the demand for increased data rates is growing in telecommunications, 6G/sub-millimeter Wave (sub-mmW) aims to achieve the desired capacity through operation at very high frequencies (~300GHz). InP-based devices are nowadays the best-in-class devices to operate efficiently at these frequencies [1]. Achieving high performance and stable ohmic contacts using CMOS-compatible metallization is a first challenge to overcome to address HBT-InP based circuits integration on large scale silicon. To obtain 6G/sub-mmW requirements such as THz Maximum Frequency of Oscillation, values in the order of 10^{-8} ohm.cm² for the specific contact resistivity are required mainly for emitter and base contacts of the transistor [2], as HBT frequency performance is directly linked to the ohmic contacts quality. Structures with dimensions as close as possible to the common THz HBTs emitter, base and collector contact dimensions are thus necessary for accurate contact evaluation.

Device description and TLM interpretation

TLM structures with contact dimensions from 5x5µm to 0.35x0.35µm are formed on integrated $In_{0.53}Ga_{0.47}As$/InP stacks on a 200mm silicon manufacturing platform (Fig. 1). Structures were first measured following the classical TLM extraction methodology. However, interpreting the resistivity results is not straightforward as the mesa geometry of our structures is incompatible with usual TLM assumptions [3]. Indeed, as the δ distance (invariant versus contact geometry) becomes significant for low contact dimensions, the global current path within the structure geometry has to be considered, see Fig. 2. To address this issue, we directly considered our contact and mesa geometries using numerical simulation (COMSOL software). Borders of the structures are considered fully isolated and resistivity induced by the contact metal stack is ignored, as it has been evaluated to be negligible. Contact resistivity and conductivity values are respectively set to the metal/semiconductor interfaces and to the semiconductor layer.

Results and discussion

To calibrate our extraction methodology, we first used our numerical model on n-type SOI stacks (Fig. 3). Initial ρ_c and R_{sh} values for simulation were taken from TLM measurements realized on the largest available contact area (5x5µm). As Fig. 3 shows, we can correctly assess the measured current levels for larger contact dimensions with the initial ρ_c and R_{sh} values. However, for smaller ones (0.35x0.35µm), significant errors appear for low spacing distance (*d*) values, meaning that these contacts are not accurately modeled. We thus adjust the ρ_c and R_{sh} values by determining how they individually affect the fitting of the curves for the 0.35x0.35µm geometry, see Fig. 4. Values providing the best overall fit along all spacing distances (*d*) are retained and reinjected into the simulation. We found out this allows to assess a single value of ρ_c and R_{sh} for all contact geometries, as less than 3.5% error is obtained between measured and simulated current levels. Our numerical solution thus properly models the contact for all dimensions. Numerically extracted R_{sh} and ρ_c are then compared with classical TLM extraction. Sheet resistivity is only modified by +4% whereas ρ_c can be over-evaluated by ~50% using classical TLM extraction methodology, depending on the contact geometry (Table 1). This confirms that classical TLM interpretation is limited for scaled contact geometries as in our case. This methodology has then be used to extract the contact resistivity of CMOS-compatible Ti-based contact on n^+-InGaAs layers. Extraction for 0.35x0.35µm contact leads to ρ_c = 7,5.10^{-8} ohm.cm² value (Fig. 5). It is 15.3% less than the value extracted using classical TLM interpretation. Such ρ_c value on n^+-InGaAs is comparable to the state-of-the-art, see Table 2. This is a convincing and encouraging result for future HBT-InP emitter and collector contacts fully integrated in silicon environment, with values of 10^{-8} ohm.cm².

Conclusion – A TLM-based numerical extraction has been proposed to properly extract the sheet resistance and contact resistivity of CMOS-compatible ohmic contacts on n-InGaAs layers. This refinement allows to reduce errors by 15.3% compared to classical TLM extraction for such scaled contacts. The obtained ρ_c value is compatible with 6G THz applications and comparable to the state-of-the-art.

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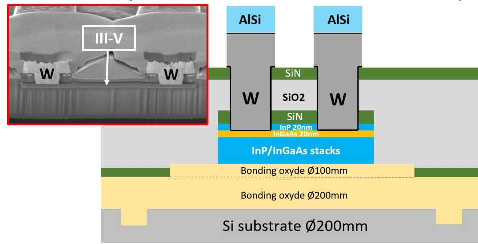

Fig. 1: Schematic view and FIB-STEM picture of the technology stack embedded in dielectrics. The Ti/TiN/W/Ti/AlSi metallization is deposited to contact the n+-InGaAs layer, doped $N_d = 5.10^{19}$ cm^{-3}.

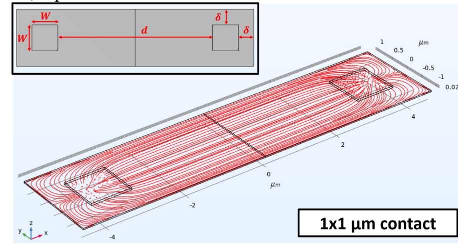

Fig. 2: Reproduction of measured ohmic contact-based structures for TLM extraction of electrical parameters with a COMSOL assisted methodology. 3D current flow is adequately assessed regarding mesa geometry (large δ distance).

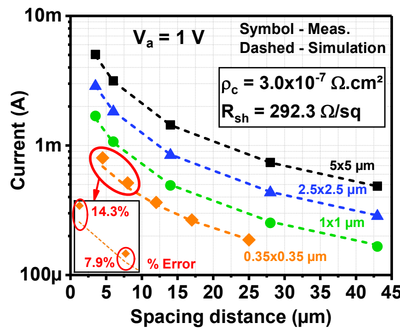

Fig. 3: Comparison of measured and simulated electric currents according to geometries. Smaller contacts (relevant for our application) are not accurately modeled using ρ_c and R_{sh} from 5x5µm contacts obtained from classical TLM analysis.

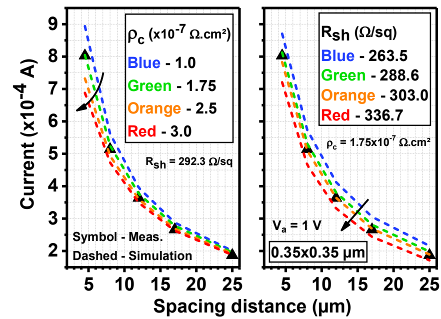

Fig. 4: Impact of ρ_c (left) and R_{sh} (right) modification on the simulated electric current curves. ρ_c affects the offset and the slope of the curves for small *d* values (left). Modifying R_{sh} (right) applies a global offset to the curves.

Methodology calibration: n-type SOI

Contact geometry (µm)	Classical TLM ρ_c extraction (10^{-7} ohm.cm²)	Simulation ρ_c extraction (10^{-7} ohm.cm²)	% Error
5 x 5	3.04	1.75	- 42.4 %
2.5 x 2.5	3.60		-51.4 %
1 x 1	2.15		- 18.4 %
0.35 x 0.35	1.84		- 4.9 %

Table 1: ρ_c extraction difference between classical TLM methodology and simulation based on n-doped SOI stacks. Large contact extraction leads to ~50% error. Our simulation allows to fit all results with only one ρ_c value.

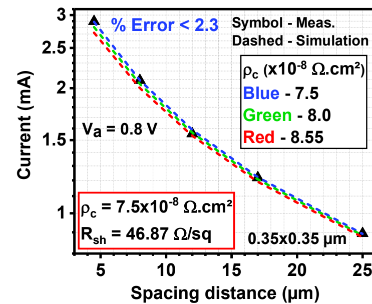

Fig. 5: ρ_c extraction (7,5.10^{-8} ohm.cm²) from ohmic contacts on n-type InGaAs in CMOS-compatible integration using our methodology. Standard TLM extraction yields 8,85.10^{-8} ohm.cm² (15.3% error).

	This work	[4]	[5]	[6]	[7]	[8]
n-InGaAs doping level (10^{19} cm^{-3})	**5.0**	~7.5	Not specified	3.0	1.0	1.0
Contact metal	**Ti (/TiN/W)**	Ti (/TiN/W)	W	Mo (/W)	Mo (/Ti/TiN/W)	Ti (/Pt/Au)
CMOS-compatible process integration	**Yes**	Yes	Yes	No	No	No
Substrate	**Si 200mm**	Si 200mm	Si 200mm	Si (Ø not specified)	Si (Ø not specified)	InP (Ø not specified)
Contact area for resistivity extraction	**0.35 x 0.35 µm**	0.05 x 2 µm	0.09 x 0.463 µm	/	/	25 x 30 µm
ρ_c (10^{-8} ohm.cm²)	**7.5**	72	7.51	0.8	~1.6	~2.0

⇨ used in **[9]**

Table 2: Benchmark of ohmic contacts on n-InGaAs. Our CMOS-compatible process yields values in line with state-of-the-art for THz HBT [8-9].