Operation of Junctionless Nanowire Transistors Down to 4.2 Kelvin

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Junctionless Nanowire Transistors (JNTs) appeared as an interesting alternative for MOSFET downscaling due to their less complex fabrication process when compared to standard inversion-mode nanowires associated with forming sharp junctions at the channel source and drain ends. Although several works discuss the operation of JNTs in different temperature ranges, the experimental operation of these devices in cryogenic temperatures down to 4.2K, which is of interest range for quantum computing, is scarce [1]. This work demonstrates the experimental results of state-of-the-art JNTs from 300K down to 4.2K obtained through DC measurements. The fundamental device parameters, such as threshold voltage (V_{TH}), inverse subthreshold slope (SS), low field mobility (μ_0), and Drain-Induced Barrier Lowering (DIBL) are presented and discussed.

The devices used in this work are n-type SOI JNTs fabricated at CEA-Leti, following the process of ref. [2]. Fig. 1 presents the measured drain current (I_{DS}) as a function of gate voltage (V_{GS}), obtained with a drain bias of V_{DS}=40mV for the devices with variable L and W_{FIN}=10nm for temperatures down to 4.2K. It is possible to see that all devices present a Zero Temperature Coefficient (ZTC) point in the I_{DS} *vs.* V_{GS} curves, related to the series resistance and its temperature dependence [3], indicating a reduced series resistance in the whole temperature range. The ZTC is shifted to slightly higher V_{GS} values and presents some dispersion when L is reduced [4]. Using the data from Fig. 1, the SS and V_{TH} are extracted and presented in Figs. 2 and 3, respectively. As expected, at room temperature the L reduction degrades the SS from 61mV/dec for the L=100nm to 68mV/dec for the L=20nm. For temperatures smaller than 100K, the SS difference to the theoretical limit increases and saturates at a minimum of around 10-20mV/dec at 4.2K, similarly to what is observed in inversion-mode (IM) nanowires, which can be linked to the presence of band tails at cryogenic temperatures [5]. The V_{TH}, extracted by the double derivative method, increases with the temperature reduction at a rate of $|dV_{TH}/dT|\approx$0.56mV/K regardless of the channel length between 300K and 100K, although the V_{TH} of the shorter device is always smaller. For temperatures smaller than 100K, the $|dV_{TH}/dT|$ rate appreciably reduces to about 0.003mV/K. This effect is associated with partial carrier ionization at the cryogenic regime, as the dV_{TH}/dT is directly proportional to the ionized N_D species [3]. Fig. 4 presents the extracted μ_0 as a function of temperature. For the L=100nm devices, the μ_0 increases from 60cm^2/V.s at 300K to 120cm^2/V.s at 4.2K. For the L=20nm device, the μ_0 increases from 20cm^2/V.s at 300K to 45cm^2/V.s at 4.2K. All our JNT present a clear dependence with T, regardless of L and W_{FIN}. In particular, the mobility is improved as T decreases, showing that impurity scattering is not the prevailing mechanism of transport. The mobility degradation regarding the channel length is associated with the neutral defects scattering in the channel and/or at the interface between the source and drain regions [6]. In Fig. 5 we plotted the DIBL of the studied devices, showing degradation at 4.2K with respect to 300K with different magnitude depending on L and W_{FIN}.

The junctionless nanowire transistors presented in this work have shown an appropriate behavior regarding the temperature reduction when it comes to their DC performance, with improvements in certain electrical parameters and coherent response to variations in channel length and fin width.

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References

[1] Renan Trevisoli et al. Semiconductor Science and Technology, v. 31, pp. 114001, 2016.

[2] S. Barraud et al., *IEEE Electron Device Letters*, vol. 33, no. 9, pp. 1225-1227, Sept. 2012.

[3] R. D. Trevisoli et al., Appl. Phys. Lett., vol. 101, no. 6, p. 062101, 2012.

[4] E. Catapano et al., IEEE Transactions on Electron Devices, v. 70, n.3, pp. 845-849, March 2023.

[5] A. Beckers, F. Jazaeri and C. Enz, IEEE Electron Device Letters, vol. 41, no. 2, pp. 276-279, Feb. 2020.

[6] M.-K. Joo et al., Semiconductor Science and Technology, v. 29, pp. 045024, 2014.

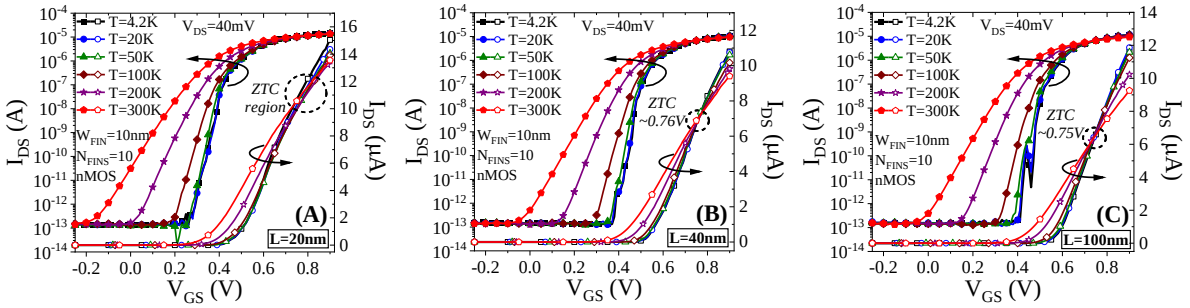

Figure 1 – Measured drain current as a function of the gate voltage, obtained with V_{DS}=40 mV, for junctionless nanowire transistors with (A) L=20nm, (B) L=40nm, and (C) L=100nm and W_{FIN}=10nm, in several temperatures from 300 Kelvin down to 4.2 Kelvin.

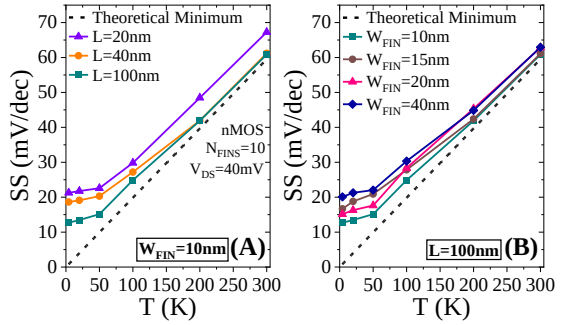

Figure 2 – Calculated subthreshold slope as a function of temperature for junctionless nanowire transistors with (A) variable channel length for W_{FIN}=10nm and (B) variable fin width for L=100nm.

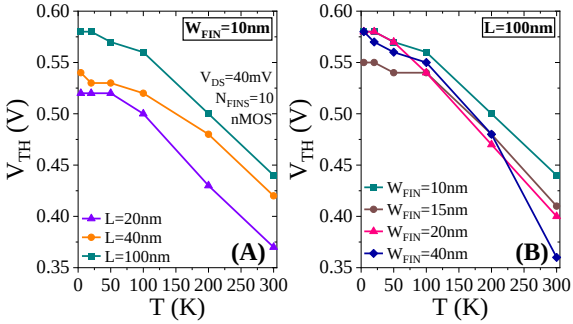

Figure 3 – Calculated threshold voltage as a function of temperature for junctionless nanowire transistors with (A) variable channel length for W_{FIN}=10nm and (B) variable fin width for L=100nm.

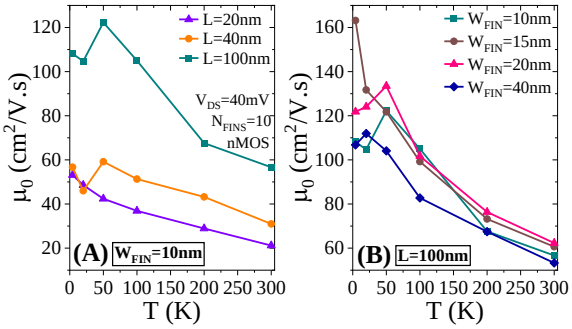

Figure 4 – Extracted low field mobility as a function of temperature for junctionless nanowire transistors with (A) variable channel length for W_{FIN}=10nm and (B) variable fin width for L=100nm.

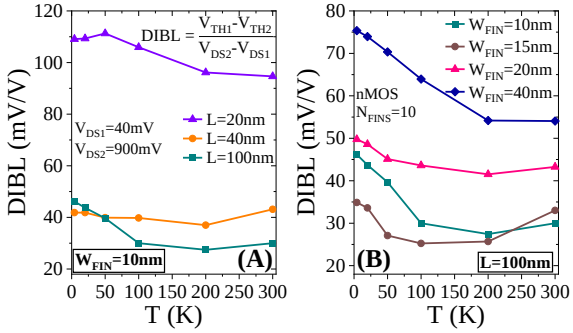

Figure 5 – Extracted drain-induced barrier lowering as a function of temperature for junctionless nanowire transistors with (A) variable channel length for W_{FIN}=10nm and (B) variable fin width for L=100nm.