Investigation on the Performance Limits of Dirac-Source FETs

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Introduction. The investigation in the area of steep-slope FETs was recently enriched by a proposal exploiting the conical band structure of graphene to control high-energy electron injection into the channel of a 2D-material based FET [1-4]. In this work, we extend the approach adopted in [3-4] by developing a two-dimensional (2D) simulation tool addressing Poisson's equation within the MoS_2 section of the DS-FET under the assumption of ballistic transport. Next, we compute the device characteristics, which are quite sensitive to the tunneling probability at the graphene-MoS_2 heterojunction. Our results confirm that a subthreshold swing SS as low as 40 mV/dec can be achieved, and that SS values below 60 mV/dec are extended up to three and a half decades.

Simulation approach. We assume a zero thickness of the semiconductor monolayer and, thus, a delta-like electron distribution. With this approach, we just need to solve Laplace equation within the oxide and use the charge density per unit area to establish the appropriate nonhomogeneous Neumann boundary condition at the semiconductor interface. As the charge density depends on the local potential, an iterative procedure is required to solve the problem. Both an SOI and a DG-FET can be treated by the code. The device characteristics are computed using Landauer's formalism with the WKB approximation for the tunneling probability. The current integration is carried out numerically on the 2D potential profile. It's worth noting that the device performances are influenced by the energy difference between the barrier height at the graphene-channel heterointerface and the Fermi level in graphene source $\phi_{SB} = E_C(0) - E_{FS}$.

Simulation results. In this investigation, the Dirac energy below the graphene control gate is set at 0.3 eV, leading to a leakage current I_{OFF} slightly below 10^{-9} A/µm at $V_{GS} = 0$ V. Fig. 1 shows the MoS_2 conduction band profiles in the transport direction for two gate lengths, namely: $L_g = 10$ nm (solid lines) and $L_g = 3$ nm (dashed lines) and different gate voltages. In both cases, a 1-nm SiO_2 gate insulator is considered. Dotted lines refer to an HfO_2 gate insulator device with the same equivalent oxide thickness (EOT). Fig. 2 represents the turn-on characteristics of the DS-FET for different values of ϕ_{SB} (solid lines). The dashed lines represent instead the device characteristics computed with the assumption of a triangular barrier with a 4-nm base width, as was done in Ref. [3]. The figure shows that the ON-state current is heavily underestimated with such a simplified potential behavior, especially for the highest energy barriers. Fig. 3 shows the turn-on characteristics and subthreshold-swing (SS) for the SiO_2 (solid lines) and for the HfO_2 (dashed lines) gate-insulated DS-FETs. Finally, Fig. 4 exhibits the turn-on curves for two different DS-FETs with gate length $L_g = 10$ nm (solid lines) and $L_g = 3$ nm (dashed lines) and the minimum SS as a function of gate length.

Conclusions. This study proves that an accurate 2D potential profile is a prerequisite for a quantitative prediction of the DS-FET potential in view of future practical applications and shows that an SS below 40 mV/dec can be achieved and sustained over 3 to 4 orders of magnitude of currents.

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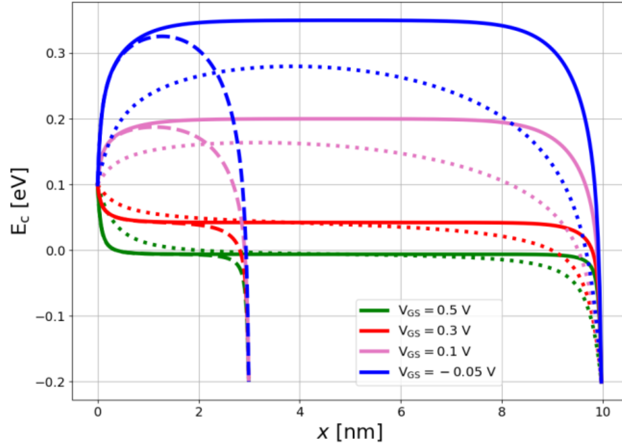


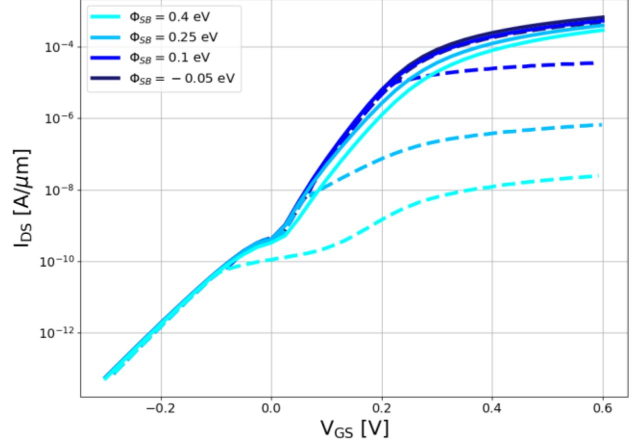
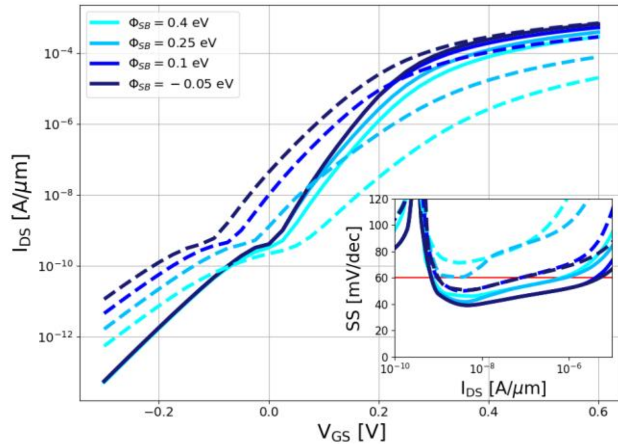


Fig. 1. Conduction band profiles in the lateral direction for two gate lengths, namely L_g = 10 nm and L_g = 3 nm and different gate voltages, ranging from -0.05 V to 0.5 V. ϕ_{SB} = 0.1 eV is assumed. Solid lines refer to a SiO_2 gate insulator having a thickness t_{ox} = 1 nm; dotted lines refer to an HfO_2 gate insulator with the same EOT. A substantial lowering of the potential barrier occurs within the channel at low gate voltages with the HfO_2 dielectric.

Fig. 2. Transfer characteristics of the DS-FET with a gate length L_g = 10 nm and a SiO_2 gate dielectric for different ϕ_{SB} values. Solid lines: present model. Dashed lines: Tunneling probability computed with the assumption of a triangular tunneling barrier with a base width of 4 nm [3]. Assuming a fixed tunneling barrier width clearly leads to an underestimation of the current, as it overstates the actual tunneling width, as shown in Figure 1.



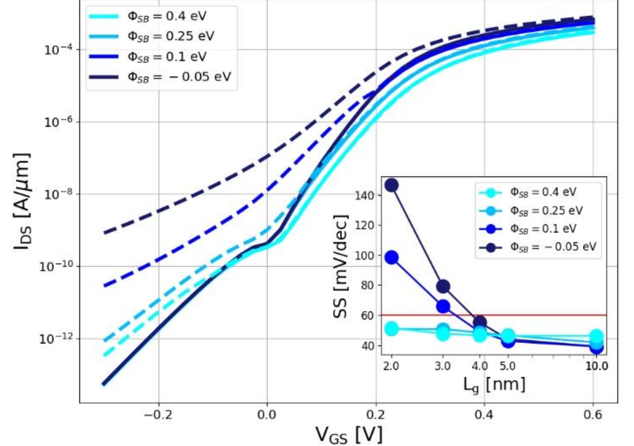


Fig. 3. Transfer characteristics of the DS-FET with a gate length L_g = 10 nm for different values of ϕ_{SB}. Solid lines: SiO_2 gate dielectric with thickness t_{ox} = 1 nm. Dashed lines: HfO_2 gate dielectric with the same EOT. Inset: SS comparison for the two devices. The use of HfO_2 as gate dielectric heavily degrades the subthreshold swing as well as the on-state current at the highest barrier heights.

Fig. 4. Transfer characteristics of the DS-FET for two gate lengths, L_g = 10 nm and L_g = 3 nm, for different values of ϕ_{SB}. Solid lines: gate length L_g = 10 nm. Dashed lines: gate length L_g = 3 nm. Inset: minimum SS as a function of gate length in semi log axes. With low gate lengths the leakage current substantially increases and the SS degrades, as for conventional MOSFET devices.

References

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