Substrate Crosstalk Characterization for optimized Isolation in FDSOI

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The continued large-scale integration of CMOS technologies has enabled complex system on chip (SoC) applications. These SoC systems often integrate a logic circuits (aggressor) along with sensitive analog and RF circuit blocks (victim). The dynamic signal switching of logic block couples through the substrate and impact the performance or functionality of the sensitive analog/RF block. The fundamentals of crosstalk between noise source and victim are well discussed in the literature. The approach for crosstalk reduction is often driven in terms of substrate resistivity (i.e., either very low (~1 mΩ.cm) [1] or high (>1 kΩ.cm)) and introduction of conductive layers in SOI system [2],[3]. It has been demonstrated that triple wells in bulk CMOS can be equal or better in isolation compared to SOI [4]. However, for mixed mode CMOS circuits, the choice of specialized substrate is not trivial. This work consolidates the solutions of crosstalk reduction in commercial SOI resistivity substrate (~1 – 100 Ω.cm) by investigating design-based solutions in fully depleted SOI (FDSOI) technology. This crosstalk study evaluates the isolation in term of SOI vs. bulk, junction impact, lateral resistance, and noise shunting elements (guard-rings). A novel guard-ring scheme deploying the combination of resistive and capacitive elements for a superior isolation is demonstrated.

The test structures are designed using 22nm FDSOI process in ground signal ground layout as shown in Fig. 1. The parameter S_{21} from 2-port S-Parameters measurement is used as a metric to evaluate crosstalk isolation. At first the reference is established for devices in bulk and SOI separated by STI as shown in Fig. 2. The STI oxide inhibit the surface coupling component between aggressor and victim which is evident with increased spacing. SOI devices exhibit significant lower crosstalk (~ -100 dB) at the lower frequency regime due to BOX indicated by the slope of 40 dB/dec until the inflection point of 3 GHz. The increase of lateral resistance can also be achieved by deploying pn junctions. In addition, a shunting path for noise signal in the form of guard-rings further reduces the crosstalk. Fig. 3 shows that for bulk devices, the introduction of a single and double pn-junction reduces the crosstalk by ~55 dB and ~80 dB at 40 MHz respectively. The bulk test structure with double junction shows 40 dB/dec slope beyond 200 MHz indicating a similar isolation to SOI integration. On the other hand, SOI devices with the resistive guard-ring show minor dependency of the pn-junctions on crosstalk magnitude and slope. For superior isolation over the wide frequency range the combine resistive and capacitive guarding can be combined as shown in Fig. 1(b). Fig. 4. demonstrate improved crosstalk isolation for mixed guard-ring at higher frequencies (> 1 GHz) while keeping the total guard ring area the same. The benefit of adding capacitive guarding to the existing resistive guarding translated to 8 dB at 10 GHz for double pn-junction. The SOI devices with MxCap guard-ring design exhibit overall the best crosstalk isolation followed up by the resistive guard-ring. The improved isolation of MxCap guard-ring compared to bulk device with resistive guard-ring is clearly observed for frequencies > 400KHz.

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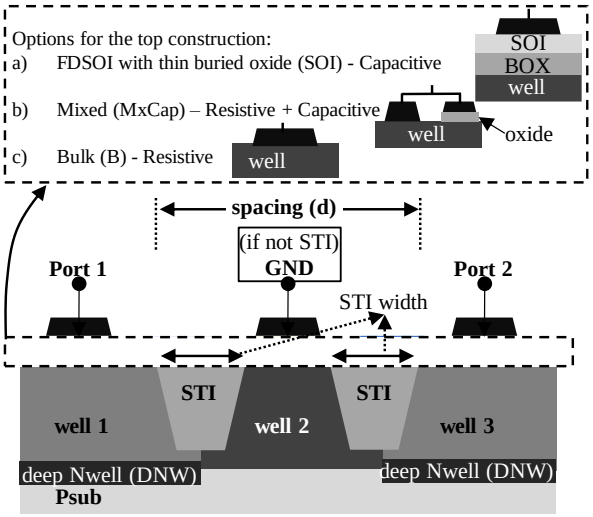

Fig. 1. Cross-section of the 2-port experimental test structures. Port 1 and port 2 can be regarded as noise source and victim devices. The center optional terminal "GND" acts as a noise-shunt or guard-ring. The design variables are: type of well (n/p-type), device type (SOI or bulk), type of guard-ring, spacing between noise source and victim.

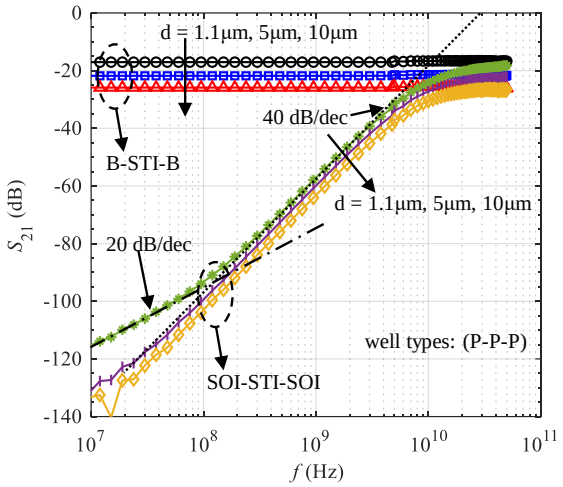

Fig. 2. S_{21} magnitude (crosstalk) vs. frequency for the structure with STI separating aggressor and victim devices. The well type are mentioned as: (well 1 – well 2 – well 3). The top construction scheme follows the convention i.e. (device type Port 1 – guard-ring – device type Port 2).

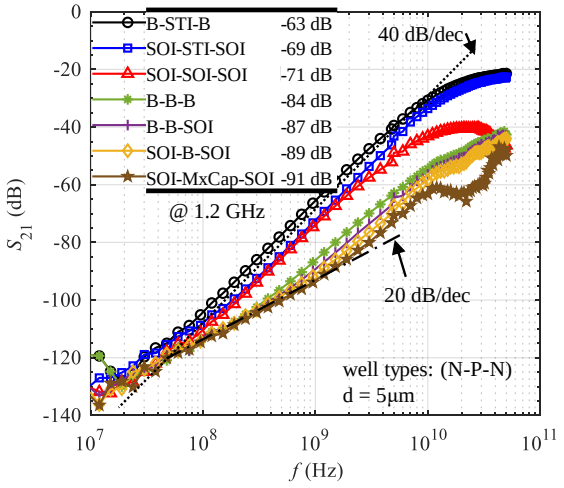

Fig. 3. Crosstalk measurement of bulk and SOI devices with resistive type guard-ring having spacing of 1.1 µm.

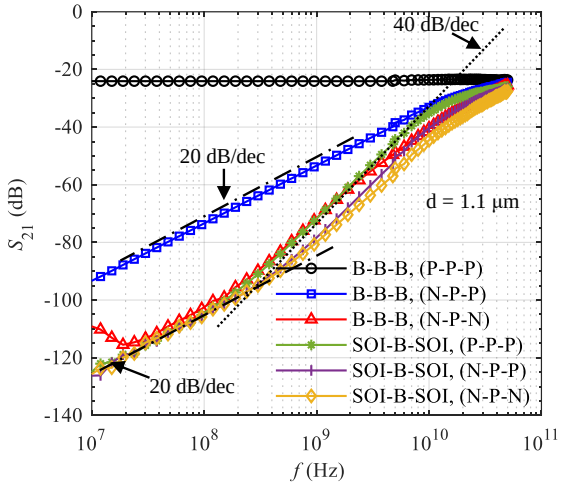

Fig. 4. Comparison of crosstalk for all top contruction of bulk and SOI type agressor/victim. The magnitude of S_{21} at the frequency of 1.2 GHz is listed in the legend table.