Interlayer Exchange Coupling for Enhanced Performance

in Spin-Transfer Torque MRAM Devices

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Spin-transfer torque magnetoresistive random access memory (STT-MRAM) is revolutionizing nonvolatile storage with its broad application and data density benefits, driven by the magnetic tunnel junction (MTJ) with a CoFeB-based structure. Despite its advantages, miniaturization introduces reliability issues like back-hopping [1]. Our research focuses on the interlayer exchange coupling (IEC) in MTJs, crucial for magnetic alignment and device performance, aiming to optimize MTJ configurations for advanced memory technologies [2].

Magnetization dynamics in spintronics is defined by the Landau-Lifshitz-Gilbert (LLG) equation. IEC, critical for these dynamics, introduces a free energy density related to the angle $\Delta \emptyset$ between adjacent layer magnetizations as $E = J_1 cos(\Delta \emptyset) - J_2 cos^2(\Delta \emptyset)$ [3]. The constants J_1 and J_2 indicate the coupling strength and type (ferromagnetic or anti-ferromagnetic). Considering only the bilinear coupling term, the above expression simplifies to $E = J_1 cos(\Delta \emptyset)$. This formulation is essential for simulating IEC effects using finite element method (FEM) simulations, guiding the boundary conditions for accurate modeling of magnetic interactions within MTJs.

Exploratory simulations on the impact of IEC on various MRAM cells, depicted in Fig. 1, indicate that the absence of coupling or the presence of strong ferromagnetic interactions between the free layers (FL) can accelerate the switching process. In contrast, antiferromagnetic coupling may decelerate this process due to the complex dynamics of interlayer interactions. These findings, as shown in Fig. 2 and Fig. 3 for the configuration in Fig. 1(a) and in Fig. 4 and 5 for the setup in Fig. 1(b), underscore the intricate influence of IEC on magnetic switching, pointing out how device performance can be optimized by adjusting the coupling strengths.

This investigation into IEC's impact on STT-MRAM devices challenges conventional views on magnetic coupling, emphasizing the need for precision in engineering IEC to boost performance. The study suggests that optimal IEC tuning can lead to faster switching, increased device reliability, and improved data retention, marking a significant step forward in the field of spintronics and memory technology optimization.

References

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Figure 1: The intricate design of a multilayered MRAM cells in a more comprehensible form. (a) and (b) display a ultra-scaled MRAM cell. Colorcoding is utilized for clear differentiation of components: the RL is marked in violet, the FL in teal, and the TB or NMS in orange. Non-magnetic (NM) contacts are represented in gray. Interfacial engineering regions are highlighted by white zigzag lines. The interaction strengths between the RL and the first FL (FL₁) and between FL₁ and the second FL (FL₂) are denoted by J_{iec_1} and J_{iec_2} , respectively.



Figure 2: Magnetization dynamics for the multilayered MRAM cell in Fig. 1(a), with a particular emphasis on the influence of IEC strengths, J_{iec_1} and J_{iec_2} , on the switching processes from AP to P. The range of coupling strengths reflects experimental findings on magnetic interactions. The left panel sets J_{iec_1} to a negative value to demonstrate its effect on switching. The middle panel offers a contrast by setting J_{iec_1} to zero, while the right panel adopts a positive J_{iec_1} to ach illustrating distinct dynamics. These simulations reveal the intricate and significant role of IEC in the switching behavior of advanced MRAM devices.



Figure 3: Magnetization dynamics during P to AP switching for the multilayer MRAM cell in Fig. 1(a), highlighting the critical role of IEC parameters, J_{icc_1} and J_{icc_2} .



Figure 4: Magnetization dynamics during AP to P, for the multilayered MRAM cell in Fig. 1(b), highlighting the critical role of IEC parameters, J_{icc_1} and J_{icc_2} .



Figure 5: Magnetization dynamics during P to AP switching for the multilayer MRAM cell in Fig. 1(b), highlighting the critical role of IEC parameters, J_{icc_1} and J_{icc_2} .