Si/$Ge_{1-x}Sn_x$/Si transistors with highly transparent Al contacts

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The introduction of GeSn as a channel material, with its modulated band structure and high carrier mobilities for both electrons and especially holes, is promising for optoelectronics and Beyond- CMOS technologies with high on-state conductance as well as low power cryogenic applications. [1] Therefore, forming high-quality contacts to the GeSn is of utmost importance. In this regard, we investigate the Al contact formation to nanosheets composed of thin $Ge_{1-x}Sn_x$ layers with Sn concentrations from 0.5% to 4%. The nanosheets are patterned from vertical Si/$Ge_{1-x}Sn_x$/Si heterostructures (Fig. 1), grown on SOI substrates by molecular beam epitaxy (MBE) at ultra-low temperatures of 175°C, adapted from the SiGe growth in [2]. Utilizing a thermally induced exchange reaction [3] between Al and Si/$Ge_{1-x}Sn_x$, monolithic metal-semiconductor-metal lateral heterostructures with abrupt Al-$Ge_{1-x}Sn_x$ junctions are formed (Fig. 2). Implemented in field-effect transistors, the electrical transport is investigated (Fig. 3), revealing linear IV-characteristics, suggesting highly transparent quasi-ohmic contacts. The transfer characteristics show a very dominant p-type conduction, which can be attributed to strong Fermi level pinning to the valance band and potentially also to hole-gas formation between the 4 nm thin $Ge_{1-x}Sn_x$ layer sandwiched vertically between two Si layers.[3] Temperature-dependent measurements indicate that at cryogenic temperatures, the $Ge_{1-x}Sn_x$ channel can be sufficiently depleted due to fewer thermally excited states at $V_G > 0$. This results in a drain current modulation over three orders of magnitude, while the on-currents remain mostly temperature-independent, making the system especially interesting for cryo-CMOS applications. The comparison of nanosheets with different stoichiometries (Fig. 4) shows that an increased Sn content enhances conductivity, over 20x higher vs. a control sample with a pure Ge layer in agreement with an accumulation channel. However, the off-state is given by depletion implying a V_G dependent overall gate capacitance accompanied with degraded I_{on}/I_{off} ratios and subthreshold slopes. To decouple the influence of the carrier injection barrier and the channel conduction, a multi-gate structure, featuring a junction gate (JG) atop the Al- $Ge_{1-x}Sn_x$ interfaces and a channel gate (CG) in the middle of the $Ge_{1-x}Sn_x$ channel, is investigated (Fig. 5). Thereby, it was found that keeping V_{JG} at -5 V and sweeping V_{CG}, the on-state resistance can be improved by a factor of ~40.

References

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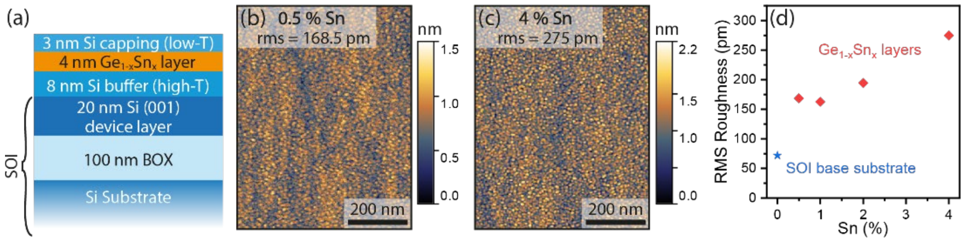

Fig. 1: (a) Schematic of the epitaxially grown Si/Ge$_{1-x}$Sn$_x$/Si heterostructure on SOI, with AFM surface topography of the substrate containing 0.5% (b) and 4% Sn (c). The root-mean-square surface roughness of four substrates with different Sn contents (0.5%, 1%, 2%, 4%) and the base SOI substrate are compared in (d).

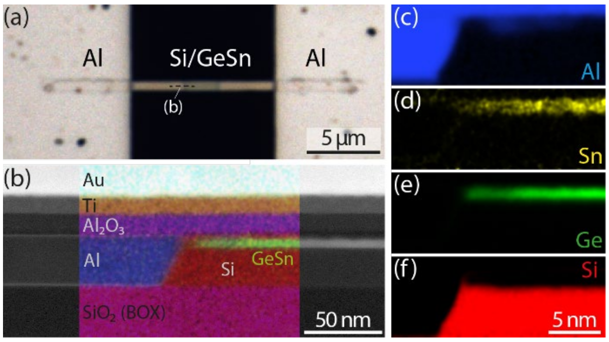

Fig. 2: (a) Microscope image of the formed Al-Si/Ge$_{0.99}$Sn$_{0.01}$ heterostructure after the thermally induced exchange reaction. (b) HAADF-STEM image with EDX overlay of the axial cut at the Al-Si/GeSn interface, indicated in (a). (c)-(f) Single elementary EDX maps.

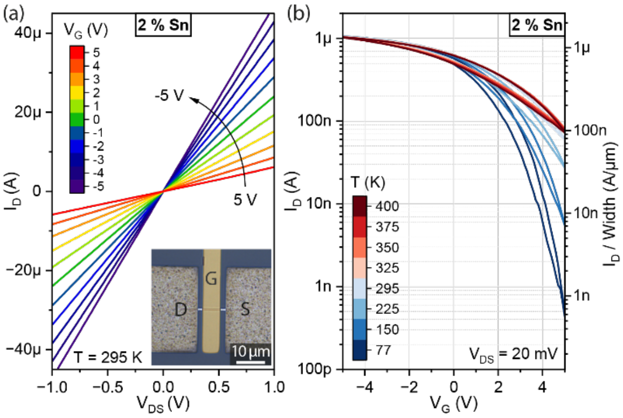

Fig. 3: (a) Linear gate dependent I/V characteristic of a top-gated Al-Ge$_{0.98}$Sn$_{0.02}$ heterostructure shown in the inset. (b) Temperature dependent transfer characteristic at V_{DS} = 20 mV.

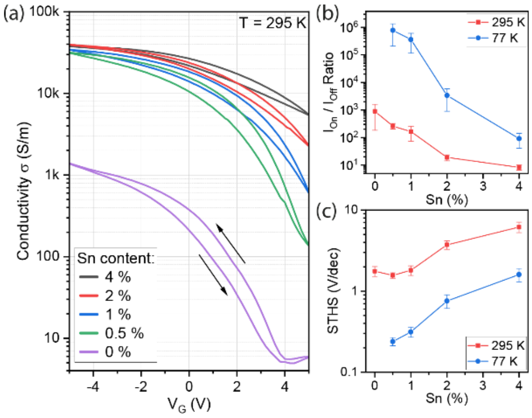

Fig. 4: (a) Comparison of the gate dependent conductivity of samples with different Sn content, including a reference sample with a pure Ge layer. (b) I_{on}/I_{off} ratio and subthreshold slope (STHS) vs Sn content, at 295 K and 77 K.

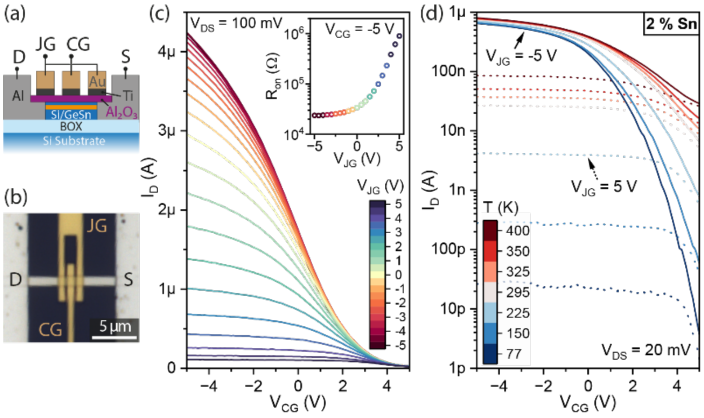

Fig. 5: (a) Schematic and (b) microscope image of a multi-gate structure with 2% Sn. Junction gate (V_{JG}) dependent transfer characteristic, with the inset showing the change in on-state resistance (R_{on}). (b) Temperature dependent transfer characteristic for V_{JG} = -5 V (solid) and V_{JG} = 5 V (dotted line).