

Enhanced Threshold Voltage Tuning in SOI MOSFET with Ferro-BOX

S. Cristoloveanu,¹ E. Nowak,² J. Barbot,² L. Grenouillet,² and I. Radu¹

¹SOITEC, Parc technologique des Fontaines, 38190 Bernin, France

²Univ. Grenoble Alpes, CEA, Leti, F-38000 Grenoble, France

Embedded in the gate stack, ferroelectric materials are of massive interest for the development of emerging sharp-switching transistor and non-volatile memory [1-2]. SOI devices feature an additional dielectric layer, the buried oxide (BOX), which can also be replaced by a ferroelectric for enriched functionality (Fig. 1a). HfO₂-based ferroelectric buried oxides (Fe-BOX) were fabricated in Popov's group and tested with the Pseudo-MOSFET method [3]. The polarization switch gives rise to two distinct non-volatile memory states.

Here, we explore a different avenue, that is the polarization-enhanced tuning of the threshold voltage in FD-SOI MOSFETs [4]. The interface coupling effect is arguably a most valuable asset of ultrathin FD-SOI technology, unheard of in FinFETs or nanowires. The rate of change of the threshold voltage with back-gate bias, derived from the equivalent circuit (Fig. 1b), is $\Delta V_T/\Delta V_{BG} = -t_{ox}/t_{box}$ [5]. The large difference between the thicknesses of the gate oxide ($t_{ox} \leq 1$ nm) and BOX ($t_{box} = 25$ nm) limits the tunability rate to 4%. Our aim is to amplify the tuning through a polarization mechanism in a Fe-BOX.

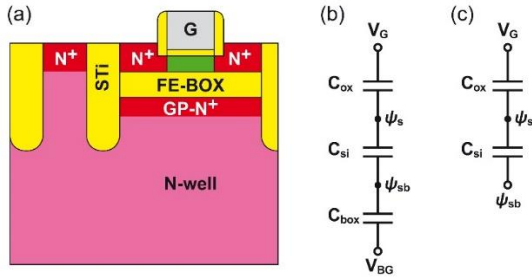


Fig. 1. (a) FD-SOI MOSFET with Ferro-BOX and equivalent circuit in subthreshold region for (b) regular BOX or (c) ferroelectric BOX.

The leading idea is to have V_{BG} acting directly on the back-surface potential ψ_{sb} at the film-BOX interface, without being absorbed by the thick BOX. This simplifies the equivalent circuit (Fig. 1c) and augments the tunability rate: $\Delta V_T/\Delta \psi_{sb} \approx -3t_{ox}/t_{si}$. In the ideal case where V_{BG} is transferred integrally via the polarization effect ($\Delta V_{BG} = \Delta \psi_{sb}$), the rate of change reaches 50% for 1 nm EOT and 6 nm thick silicon body.

Proof-of-concept simulations were performed with Synopsys tools. The n-channel MOSFET structure (Fig. 1a) comprises a gate stack with 2 nm equivalent oxide thickness, a 7 nm thick undoped body, a 10 nm thick hafnium–zirconium oxide (HZO) BOX, and raised source and drain. The gate length, the doping of the ground plane and the programming pulse applied on the back gate are variable parameters. A remanent polarization of 40 $\mu\text{C}/\text{cm}^2$ and a coercive field of 1.5 MV/cm are considered.

Figure 2a shows that even with a modest program voltage, a remarkable V_T lowering is achieved. The V_T shift reaches 1 V after 1.5 V pulse. This performance is to be compared with only 60 mV shift for a regular 25 nm BOX. For effectiveness, the ground-plane should be heavily doped ($N_D > 2 \times 10^{19} \text{ cm}^{-3}$), otherwise the series resistance absorbs part of the impulse (Fig. 2a). The initial value of the threshold voltage is recovered with a negative pulse (-6 V in Fig. 2b),

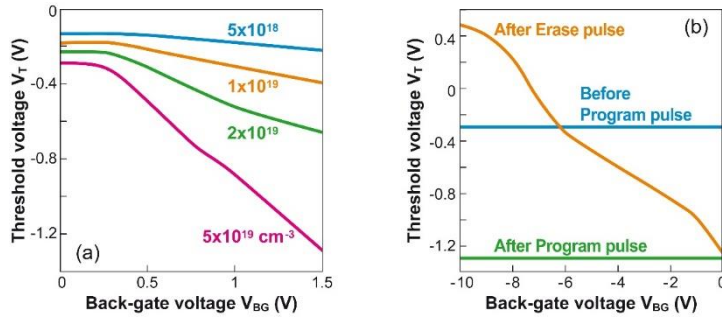


Fig. 2. (a) Threshold voltage lowering versus pulse amplitude. (b) Recovery of the initial V_T after a negative erase pulse.

In Figure 3, the gate length is scaled from 100 nm down to 18 nm. The beneficial effect of polarization is persistent and, interestingly, becomes stronger in very short transistors. In order to minimize the trap density, we have tested the option of capping the HZO layer with SiO_2 . In such a composite Fe-BOX ($\text{SiO}_2\text{-HZO-SiO}_2$), the polarization effect remains substantial provided the cap is not too thick.

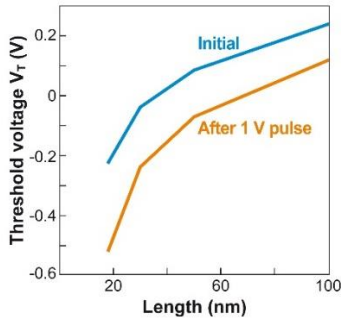


Fig. 3. Threshold voltage before and after programing versus gate length. The program pulse (1 V) and the ground-plane doping ($N_D = 2 \times 10^{19} \text{ cm}^{-3}$) are lower than in Fig. 2.

In summary, the replacement of a regular ‘passive’ BOX with an ‘active’ ferroelectric oxide is a tremendous opportunity for enhancing what is unique in FD-SOI devices, that is the dynamic control of the threshold voltage. Preliminary results confirm our concept and demonstrate that polarization effect increases the coupling rate by one order of magnitude. In addition, polarization-assisted back-biasing is a non-volatile mechanism, meaning that there is no need to maintain a constant back-gate voltage, one short pulse is sufficient. Since polarization switch is very fast ($< 1 \text{ ns}$), the principle of Fe-BOX is applicable to RF circuits.

References

- [1] J. Silva, R. Alcalá, U. Avci, N. Barrett et al, Roadmap on ferroelectric hafnia- and zirconia-based materials and devices, *APL Materials*, vol. 11(8) (2023) 089201.
- [2] J.C. Wong and S. Salahuddin, Negative capacitance transistors, *Proc. IEEE*, 2019, vol. 107(1), 49–62 (2019).
- [3] V.P. Popov et al, Ferroelectric properties of SOS and SOI pseudo-MOSFETs with HfO_2 interlayers, *Solid-State Electronics*, vol. 159(9), 63-70 (2022).
- [4] I. Radu, G. Besnard and S. Cristoloveanu, Substrat de type semi-conducteur sur isolant pour un transistor à effet de champ à capacité négative, patent FR3120983A1 (2022).
- [5] H-K. Lim and J.G. Fossum, Threshold voltage of thin-film silicon-on-insulator (SOI) MOSFETs, *IEEE Trans. Electron Devices*, vol. ED–30, 1244 (1983).