Preliminary results on industrial 28nm FD-SOI phase change memory at cryogenic temperature

Philippe Galy[1], Joao Henrique Quintino Palhares[1,2,3,4], Lorena Anghel[2], Yann Beilliard[3,4,5], Fabien Alibart[4,5], Dominique Drouin[3,4,5] J. Sandrini[1], F. Arnaud[1].

[1] STMicroelectronics, 850 rue Jean Monnet, 38920 Crolles, France
[2] Université Grenoble Alpes, CNRS, Grenoble INP, SPINTEC Grenoble, France
[3] Institut quantique, Université de Sherbrooke, 2500 Boulevard de l'Université, Sherbrooke QC J1K 2R1, Canada
[4] Laboratoire Nanotechnologies Nanosystèmes (LN2) CNRS UMI-3463—3IT, CNRS, Sherbrooke J1K 0A5, Canada
[5] Institut Interdisciplinaire d'Innovation Technologique (3IT), Université de Sherbrooke, Sherbrooke J1K 0A5, Canada.

Abstract:
This study reports new preliminary results on pulse programmed 28 nm FD-SOI UTBB fully co-integrated phase change memories (PCM) at room (RT) and cryogenic temperatures (CT). The PCM is found to be functional at 77K featuring multi-state switching with no extra operating requirements compared to RT. As the phase change memory is temperature dependent, drift tests are carried out to track the resistance change overtime subsequent to pulse programming to estimate the drift coefficients. A striking feature is that using the same programming conditions, the drift coefficient is 3 times lower at 77K with improvement on I_{on}/I_{off} ratio. These results are encouraging and open the door for PCM in cryogenic applications.

Keywords- FD-SOI CMOS, phase change memory, cryogenic temperatures

I. INTRODUCTION

In the fields of quantum, avionics, space applications or detectors in astrophysics/medicine and accelerators, cryogenic temperature is a key parameter with a wide low temperature range down to mK. Depending on the system architecture and temperature distribution, the choice of electronic control technology is very important. One of the promising candidates is FD-SOI technology which today demonstrates relevant performances, particularly in low power consumption, for analog/digital design. That's why 28nm platform devices are based on STMicroelectronics' standard 28nm ultra-thin body buried oxide (UTBB) fully depleted silicon-on-insulator (FD-SOI) technology. These devices are explored under cryogenic temperature conditions. Thus, the industrial process has been shown to be functional down to 20 mK without additional process steps. Figure 1 recalls the thin hybrid silicon film substrate and gives the $I_{ds}(V_{gs})$ from room temperature to 20 mK. This demonstrates the exceptional subthreshold slope around 2 mV/decade at 20 mK. It is also reported that the thermal offset Vt is corrected by the back gate control for P and NMOS transistors. Additionally, Phase Change Memory (PCM) is offered in the platform to deliver emerging non-volatile memories (eNVM) functionality. Figure 2 gives the design principle of 1T1R memory, a typical PCM layout where an SEM cross section represents the architecture and material types. Additionally, the phase of the material is also shown to highlight the forming, set and reset configuration based on electronics set up control. After this overview of the context, the novelty of this study is to demonstrate that with the initial configuration, it is possible to program the PCM in binary and/or multilevel mode at cryogenic temperature with no extra operating requirements. For this first investigation, the thermal condition selected is 77K. Figure 3 gives several views of the cryo-probe station test setup and the pulse programming scheme used to perform multilevel switching by means of a Keysight (Agilent) B1500A Analyzer. Binary states (high resistance state (HRS) and low resistance state (LRS)) and intermediate states are obtained at room temperature. The incremental switching using the programming sequence depicted in figure 3 consists of 10 constant amplitude SET pulses of 1.5V and 10 subsequent RESET pulses with incrementing amplitudes ranging from 1.8V to 2.7V. The pulse format remains consistent for both set and reset, with uniform rise, plateau, and fall times of approximately 70ns. The sequence is executed across BL with a steady 1.3V bias applied to WL. Each pulse is followed by 0.1V reading pulse. Figure 4a) and b) present the IV DC sweep measurements at HRS with fixed V_{WL} bias at RT (300 K) and at 77K. The corresponding fitting of Poole-Frenkel conduction dependence is also presented. As expected, we observe a considerable increase in HRS at cryogenic temperatures. Next, the set/reset incremental pulse programing sequence is applied to reach four states at RT and CT. The density distribution of resistance states achieved with 4 selected different programming steps over more than 100 pulses are reported in figure 4. Although the LRS range is the same regardless of the temperature, the HRS and intermediate resistance states (IRS) are higher at 77K Thus, it is possible to reduce the V_{BL} voltage requirements at 77k and still obtain the same resistance range and ON/OFF ratio as at RT that conversely requires a voltage of 2.7V to reach full switching range. This means that standard thick gate oxide MOS transistors could be used for the design of the selector. Figure 5 shows the temporal evolution of PCM resistance after programming and the drift model used to extract the drift coefficients (υ) of the four-state resistance at RT and 77k. Note that the states are read at 0.1 V to avoid additional self-heating in cryogenic conditions compared to 0.2 V. The drift is reduced by 3 times at 77K compared to the thermal condition of 300K. In conclusion, we report for the first time the demonstration that it is possible to program and read the PCM performing binary or multilevel switching with the same standard set up configuration at 300K and 77k. Additionally, the 28 nm FD-SOI PCM demonstrates reduced drift at cryogenic temperatures(77K). It is recalled here that this PCM (GST type) is manufactured using an industrial steps process. This study opens the door to push the limit of the cryogenic temperature where the eNVM proves to be functional. The same trend is expected to be observed on next generation nodes, for example in 18nm.

ACKNOWLEDGMENTS

The authors of this article would like to thank all colleagues at STMicroelectronics and 3IT/IQ who contributed to these results within the standard 28 nmFD-SOI process.

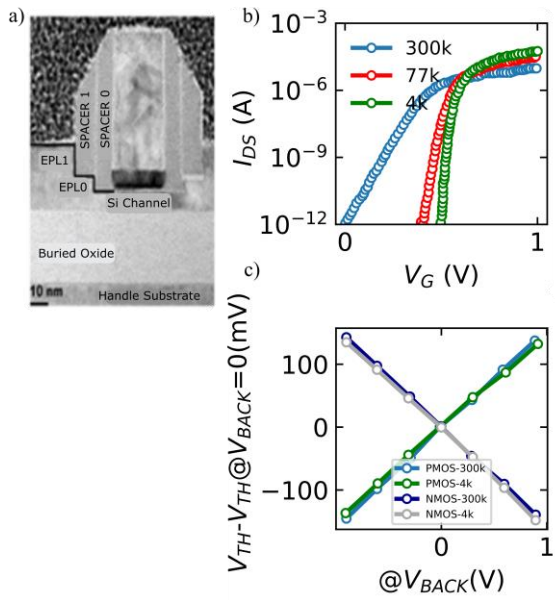

Figure 1: a) FD-SOI substrate cross section, b) $I_{ds}(V_{gs})$ for various temperatures down to 4K and c) Back Bias V_T correction for N/P MOS transistors.

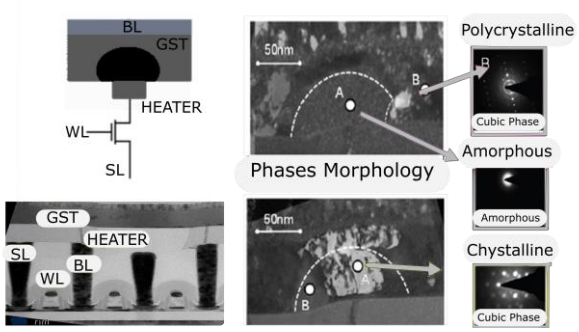

Figure 2: a) 1T1R PCM (GST material), typical Layout in 28 nm FD-SOI. PCM phases and wall PCM SEM cross section with heater and contact are depicted.

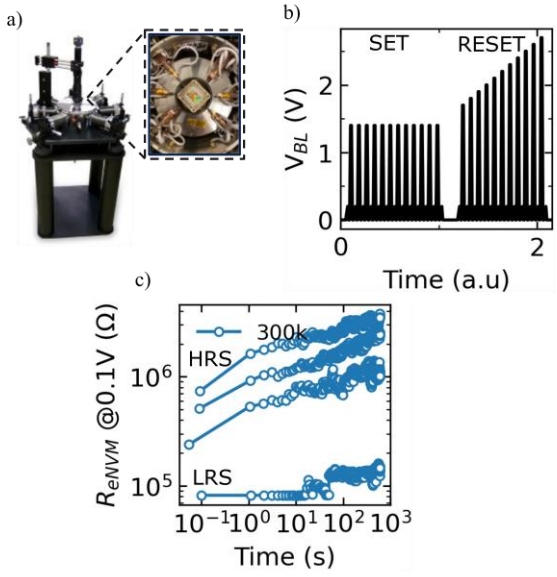

Figure 3: a) Cryogenic test setup for b) incremental set/reset pulse programming. c) Time retention at 300k up to 600s for four multilevel states corresponding to a set of selected steps within the entire programming sequence consisting of 10 SET and 10 RESET pulses (average across 10 complete sequence repetitions) (at RT.).

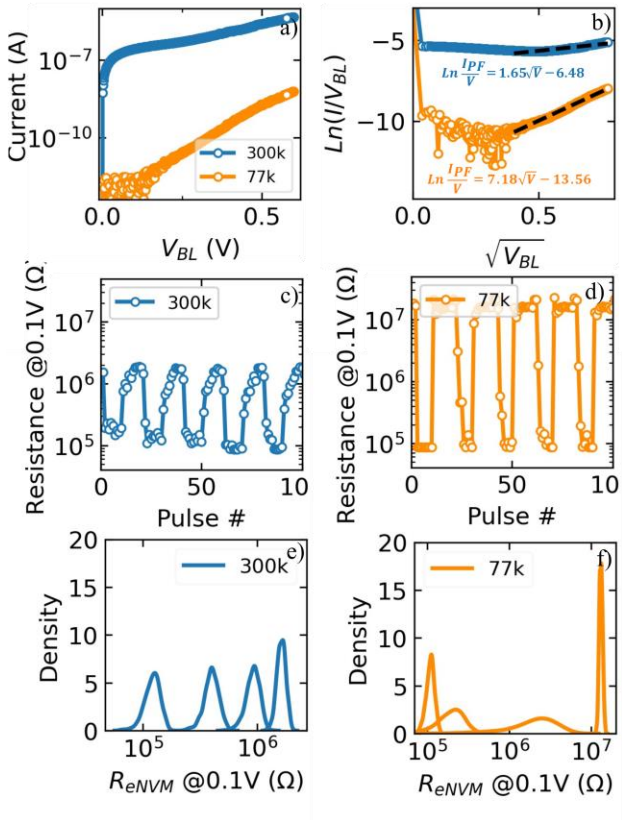

Figure 4: a) PCM IV DC sweep measurements at 300K and 77K (@HRS) and b) the corresponding fitting of Poole-Frenkel conduction dependence; c) A resistance sequence is pulse-programmed at both 300K and d) 77K, e) depicting the multilevel resistance states distribution for four selected programming steps repeated over time at 300k and f) 77k.

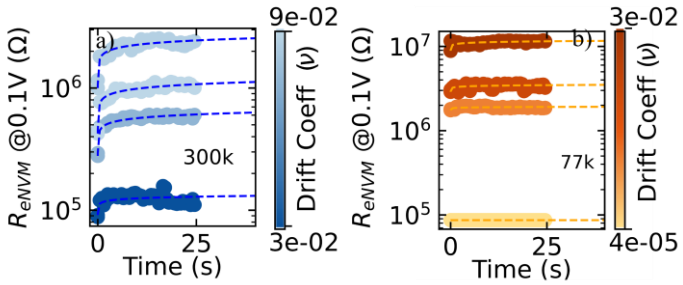

Figure 5: Time retention measurements and drift coefficient (ν) estimation according to drift model $R_t = R_{t0}(t/t_0)^{\upsilon}$ for 4 different states programmed at a) 300 and b)77K. First reading t_0 is at 0.9ms.

References:

[1] Ph. Galy et al « Cryogenic temperature characterization of a 28 nm FD-SOI dedicated structure for advanced CMOS and quantum technologies co-integration". IEEE Journal Electron Device Society, JEDS 2018. DOI 10.1109/JEDS.2018.2828465

[2] F. Arnaud et al "Enhanced Phase Change Memory Cell in 28nm FDSOI Technology for Automotive Micro-Controller Applications" - IEDM 2020.

[3] M. Casse et al : "Evidence of 2D Intersubband Scattering in Thin Film Fully Depleted Silicon-On-Insulator Transistors Operating at 4.2K".APL 2020. DOI: 10.1063/5.0007100.

[4] B. Cardoso Paz1 et al "Front and back channels coupling and transport on 28 nm FD-SOI MOSFETs down to liquid-He temperature".SSE 2021.

[5] Joao Henrique Quintino Palhares et al » A tunable and versatile 28nm FD-SOI crossbar output circuit for low power analog SNN inference with eNVM synapse ". SSE 2023.

[6] B. Quentin et al « RF performances at cryogenic temperatures of inductances integrated in a FDSOI technology«. SSE 2021

[7] D. Ielmini, "Physical interpretation, modeling and impact on phase change memory (PCM) reliability of resistance drift due to chalcogenide structural relaxation," 2007 IEEE IEDM

[8] Shih Y. H.. IEDM Tech. Dig., 2009 753, Washington, DC, USA, 2007, pp. 939-942.

[9] F. Arnaud et al "Truly Innovative 28nm FDSOI Technology for Automotive Microcontroller Applications embedding 16MB Phase Change Memory". IEDM 2018